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QUARTERLY PROGRESS REPORT

FOR

THE RESEARCH AND DEVELOPMENT

HIGH CURRENT AND HIGH VOLTAGE SILICON CONTROLLED RECTIFIERS

THIS REPORT COVERS THE PERIOD

1 JANUARY 1963 TO 31 MARCH 1963

RECTIFIER

COMPONENTS



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1 JANUARY 1963 TO 31 VARCH 1963

RECTIFIER COMPONENTS DEPARTMENT
GENERAL ELECTRIC COMPANY
WEST GENESEE STREET
AUBURN, NEW YORK

NAVY DEPARTMENT BUREAU OF SHIPS ELECTRONICS DIVISIONS

CONTRACT NUMBER: NObsr-87648
PROJECT SERIAL NUMBER: SF-013-11-05
CONTRACT DATE: 30 JUNE 1962

ABSTRACT

A study of the relationship between SCR design parameters and electrical characteristics has been made and a discussion of the pertinent points is presented.

A computer analysis of the affects of differing sizes of internal emitter shorts has been completed and is summerized.

A number of the test procedures and the nomenclature which is used are included.

PART I

1.1 Purpose

The research and development being conducted under the provisions of this contract is directed toward the development of two silicon controlled rectifiers. The first, Device B, is a 70 ampere, 1000 volt device. The other, Device C, is a 155 ampere, 1300 volt controlled rectifier. Specification objectives for these two devices are given in Table 1 (page 2, PART 1).

		DEVICE	JE B	DEVICE C	
CHARACTERISTIC	SYMBOL	CONDITION	VALUE	CONDITION	VALUE
Average Forward Current (Min.)	01	T _C - 90°C (Note 1)	70 amps.	180° half sine wave condition T_{C} - $80^{\circ}C$	155 amps.
Peak Surge Current (Min.)	I _{FM} (surge)	(Note 1)	1000 amps.	A non-recurrent of 180° half sine wave conduction immediately preceeded and followed by $\mathbf{I}_0 = 155$ amps.	2500 amps.
Peak Forward and Peak Reverse Blocking Voltage (Min,)	V FOM VROM	(Note 1)	1000 volts	Over the workable temperature range of the device	1300 volts
Turn-Off Time (Max.)	toff	(Note 1)	20 µ sec	Initially at 155 amps into resistive load with mounting interface surface at 80°C steady state (Fig. 10, MIL-S-19500/204)	25 µ sec
Turn-On Time (Max.)	t G on	(Note 1)	15 µ sec	Turn-on with a square wave gate current pulse. Io may be limited to 50 amps. through non-inductive load (Fig. 12, MIL-S-19500/204)	15 µ sec
Rate of Rise of Anode to Cathode voltage (Min)	$\frac{d(\mathbf{v_{FO}})}{dt} \text{ or }$ $d\mathbf{v}/dt$	(Note 1)	20 v/µ sec (Note 2)	Test circuit similar to Fig. 11, ML-S-19500/204 shall be used, (T _A = 125°C)	200 v/μ sec
Peak Reverse Surge Power (non-repetitive)	P _{ROM} (surge)			100 microsecond sinusoidal current pulse at 25°C.	10 K watts

Notes: 1) The requirements of MIL-S-19500/204 shall apply to the extent practicable.

2) This is an important characteristic in the design of static inverters, and warrants reasonable effort toward improvement consistent with the primary objectives of current and voltage.

Table 1 - Device specifications

2.1 GENERAL FACTUAL DATA

2.1.1 Identification of Technical Personnel

The names of engineers and technicians, together with a summary of the manhours of work performed for each device, are as listed below.

PROJECT DIRECTOR - F.E. Gentry, Manager - Advance Engineering

(a) Device B

Engineers	Technicians
R. Knaus	M. C. Brown
	K. B. Catchpole
	M. H. Curtin
	M. H. Lindner
	A. L. Smith

(b) <u>Device C</u>

Engineers	<u>Technicians</u>
R. L. Davies	A. Bolger
R. Kokosa	J. Brunner
R. P. Lyon	J. B. Crooks
	B. Tuft
	M. Yaworsky

(c) Manhours

Engineers	Technicians
942	3778

2.1.2 References

See attached sheets, pages 4 and 5, PART I.

2.1.3 Tables and Illustrations

All tables and illustrations referenced in PART I of this Quarterly Report and not included therein are appended to PART III of this Report.

REFERENCES

- R. Emeis and A. Herlet, "The Blocking Capability of Alloyed Silicon Power Transistors", Proceedings of I.R.E., Vol. 46, June 1958, pp. 1216-20.
- D. K. Bisson and R. F. Dyer, "A Silicon Controlled Rectifier", A.I.E.E. Transactions, Vol. 78, Part I.
- 3) W. B. Green, "A Fatigue-Free Silicon Device Structure", A.I.E.E. Transactions, Vol. 54, Part I, May 1961, pp. 186-91.
- 4) H. W. Henkels, "The Fused Silicon Rectifier", A.I.E.E. Transactions, Vol. 75, Part I, 1956, pp. 733-46.
- 5) N. Mapham, "The Rating of SCR's When Switching into High Currents", A.I.E.E. Conference Paper, CP63-498, I.E.E.E. Winter General Meeting, Jan. 27 Feb. 1, 1963.
- 6) G. E. McDuffie and W. L. Chadwell, "An Investigation of the Dynamic Switching Properties of Four Layer Diodes", A.I.E.E. Conference Paper CP59-671.
- 7) F. W. Gutzwiller et al, <u>Silicon Controlled Rectifier Manual</u>, Rectifier Components Department, General Electric Company, 1961, pp. 26-27.
- 8) J. L. Moll, M. Tanenbaum, J. M. Goldey and N. Holonyak, "P-N-P-N Transistor Switches", Proceedings of I.R. E., Vol. 44, Sept. 1956, pp. 1174-82.
- 9) R. W. Aldrich and N. Holonyak, Jr., "Two-Terminal Asymmetrical Silicon Negative Resistance Switches", Journal of Applied Physics, Vol. 30, Nov. 1959, pp. 1819-24.
- 10) A. N. Baker, J. M. Goldey and I. M. Ross, "Recovery Time of PNPN Diodes", I.R.E. Wescon Convention Record, Part 3, Aug. 18-21, 1959 pp. 43-7.
- 11) R. F. Dyer and G. K. Houghton, "Turn-Off Time Characterization and Measurement of Silicon Controlled Rectifiers", A.I.E.E. Conference Paper, CP61-301.
- 12) W. Shockley, "The Theory of P-N Junctions in Semiconductors and P-N Junction Transistors", Bell System Technical Journal, Vol. 28, Jul. 1949.

- 13) E. L. Steele, "Theory of Alpha for P-N-P Diffused Junction Transistors", Proceedings of I.R.E., Vol. 40, Nov. 1952.
- 14) C. T. Sah, R. N. Noyce and W. Shockley, "Carrier Generation and Recombination in P-N Junctions and P-N Junction Characteristics", Proceedings of I.R.E., Vol. 45, No. 9, Sept. 1957.
- 15) R. Beaufoy and J. J. Sparkes, "The Junction Transistor as a Charge-Controlled Device", Proceedings of I.R.E, Dec. 1957.
- 16) I. M. Mackintosh, "The Electrical Characteristics of Silicon PNPN Triodes", Proceedings of I.R.E., Vol. 46, June 1958.
- 17) J. J. Ebers, "Alloyed Junction Avalanche Transistors", Bell System Technical Journal, Vol. 34, Sept. 1955.
- 18) M. A. Melahy, "Minimum Time for Turn-Off in Four-Layer Diodes", Proceedings of I.R.E., Vol. 49, No. 9, Sept. 1961, pp. 1424.
- 19) J. C. Irvin, "Resistivity of Bulk Silicon and of Diffused Layers in Silicon", Bell System Technical Journal, Vol. 41, Mar. 1962.

2.1.4 Conferences

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On April 12, 1963, R. Wade, Bureau of Ships, Washington D. C. and C. Marcus, Naval Material Laboratory, Brooklyn, New York, visited Auburn, New York, for discussions with F. Gentry, R. Knaus, R. Lyon, B. Tuft and R. Davies. The status of Devices "B" and "C" was reviewed and new courses of action planned. Turn-off time was given particular attention.

As specified in the contract, turn-off time is to be measured according to MIL-S-19500/204. However, it was agreed that it would be very desirable to have Device B meet a turn-off time specification of 20 microseconds with the forward voltage of 1000 volts reapplied at a rate of 20 volts per microseconds. Consequently, it was decided that the delivery schedule for Device B, design samples and final report, should be extended by two months in an attempt to meet this criteria.

3.1.1 Statement of the Problem (General)

Both devices, B and C, are very high voltage silicon controlled rectifiers which must be optimized to achieve high speed and moderately high currents. Many of the characteristics are interrelated and, as a consequence, the design changes which result in lower power dissipation often are in direct conflict with those required for high speed and high voltage. A simplified summary of some of the design parameters for each characteristic are given in the following paragraphs.

3.1.1.1 Voltage

The blocking voltage capability of a silicon controlled rectifier is determined by the following factors:

- 1) The electric field within the body of the blocking junction.
- 2) The "effective" base widths and lifetime of minority carriers in those regions of the device contributing to transistor action.
- The emitter efficiency of the injecting junctions at low current density levels.
- 4) The stability and breakdown voltage capability of the surface. The breakover voltage of a silicon controlled rectifier is related to device design parameters by the equation

$$V = V_{(BR)} (1 - \alpha_{PNP} - \alpha_{NPN})^{\frac{1}{m}}$$
 (1)

where m has a value between 3 and 6, depending upon the breakdown voltage and junction impurity gradient. α_{PNF} and α_{NPN} are the current gain factors for the PNP and NPN transistor positions of the device. As an example, consider the structure shown in Figure 1. With the application of forward voltage, junction J2 becomes the blocking junction. If the junctions were of a step junction nature then the space charge layer width will be given by the relation

$$W_{SC} = K_1 \sqrt{\frac{V}{N_1}}$$
 (2)

where K_1 is constant, V the applied voltage and N_1 the number of impurities on the high resistivity side of the junction. Thus, as the number of donor or acceptor impurities on the high resistivity side of the junction increases, the depletion region width at the blocking junction decreases and the electric field increases. As a consequence, the alphas of both sections of the device increase, with that portion containing the high resistivity base region increasing more rapidly. When the sum of the alphas are equivalent to unity the breakover voltage is reached. Avalanche breakdown will occur when the relationship

$$V_{BD} \cong K_2^{N_I}^{-n} \tag{3}$$

is satisfied. For silicon, $K_2 = 5.6 \times 10^{13}$ and n = 3/4 for voltages in excess of 100 volts. If it is assumed that the device is to operate at some fraction F of the avalanche voltage then using Equations (2) and (3), the space charge width for a junction optimized for high voltage becomes

$$W_{SC} \cong K_1(FK_2) \stackrel{-\frac{1}{2}n}{(V)}$$
 (4)

Note that the width of the depletion region increases rapidly with increasing voltage. This factor has several implications. It requires wider base widths in the high resistivity section of the device in order to prevent the effective base width, W_B, from becoming zero which will result in "punch-through" by the depletion region. Although such a condition is not destructive, punch-through will cause the device to switch to the conducting state.

The conditions mentioned above relate to breakover voltage for internal body effects. Surface breakdown plays a strong role in determining the structure which can be used at high voltage. To avoid surface degredation, or surface breakdown, the electric field at the junction to surface interface must be made quite low as compared to that within the body of the device. This requirement is obvious since the filicon lattice is badly disrupted in the vicinity of a surface. As a consequence a lower voltage gradient is required to cause avalanche at the surface than within the body of the junction. Moreover, if avalanche does occur at a surface, it is very likely to result in permanent damage since it is

virtually impossible to obtain a surface sufficiently homogeneous to prevent localized breakdown. The heat generated as a result of localized breakdown is usually sufficient to cause permanent damage to the blocking characteristic

Since the electric field at the surface edge of a p-n junction is strongly affected by the surface contour in the vicinity of the depletion region, the shape and impurity concentration gradients near the surface must be carefully designed to provide a low surface field. These requirements tend to seriously limit the structural dimensions which can be used within the body of the device.

Two distinct disadvantages accompany high voltage devices. With the wider base width required, higher minority carrier lifetime is essential if the forward conducting drop is to reamin as low as that usually found in lower voltage devices. An increase in minority carrier lifetime will result in longer turn-off times as will be discussed in a later section. If the forward conducting drop is permitted to rise, the heat dissipated will rise also, and in addition the surge current capability will diminish. Secondly, the time required for turn-on will increase with wider base regions.

3.1.1.2 Current

High current applications necessitate large pnpn devices with large junction areas. A number of problems arise as the junction area is increased. Some of the more troublesome ones are:

- 1) Junction cooling
- 2) Mechanical and thermal stresses
- 3) Thermal fatigue
- 4) Maintaining parellel, uniform junctions
- 5) Non-uniform current density during turn on

The current through a reverse biased p-n junction increases exponentially with increasing temperature. Unless the blocking current is kept low, severe heating will occur resulting in thermal runaway. As a consequence, attention is focused on maintaining the junction as cool as is practical. To minimize the junction to heat-sink temperature drop, the semiconductor

junctions must not be separated from the heat-sink by any more material than is absolutely necessary. This requires either a solder which can be plastically deformed during temperature cycling or a hard solder and transition plates to prevent the silicon from fracturing due to stress. Since this device is to be used in military applications a hard solder is highly desirable, even though thicker transition plates than would be necessary for a soft solder design are required. By the use of "hard solders" the thermal fatigue problem can be overcome. A "hard solder" is one which is not strained beyond its elastic limits during cyclical operation. To use such a solder requires the use of transition plates, such as molybdenum or tungsten which have a high thermal conductivity, a high modulus of elasticity and a coefficient of thermal expansion near that of silicon. To keep the thermal resistance as low as possible, the transition plate must be made thin. Becuase the solder solidifies at high temperature during fabrication, mechanical stress builds up as the temperature is lowered due to the differences in thermal contraction of the copper heat sink, the semiconductor and its transition plate. Thus, the semiconductor material is mechanically strained. The problem then becomes one of selecting the transition plate between the pnpn device and the heat sink, such that it is thin enough for good thermal resistance yet thick enough to prevent the semiconductor material from fracturing at the low end of the operating temperature range. 4 In addition, the transition plate on top of the semiconductor should generally be thinner than the bottom one to minimize the strain in the device. This construction is illustrated in Figure 2. Thus, one finds that the larger the area of the device the thicker the bottom transition plate must be. One consequence of this is that thermal resistance per unit current density does not drop linearly with increasing junction area.

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Another serious problem with large area, three-therminal, pnpn devices is one of non-uniform current distribution during the period when the device is switching to the conducting state. 5 This problem commonly referred to as the dI/dt effect becomes more troublesome on high voltage

devices because of the increased transient times resulting from wide base widths.

3.1.1.3 dv/dt - Rate of Rise of Reapplied Forward Voltage

The dv/dt capability of an SCR is controlled by the following factors.

- The effective emitter efficiency of the emitter junctions at low current density levels.
- 2) The "effective" base widths and lifetimes of minority carriers within the device.
- 3) The capacitance of the center junction.
- 4) The uniformity of the junction.

The dv/dt effect in an SCR can be observed by applying a rapidly rising voltage across the structure in the forward blocking direction. ^{6,7} If the voltage pulse is of sufficient magnitude and has a sufficiently steep wave front, or dv/dt, then the device will switch to the conducting state. This phenomenon can be particularly troublesome when pnpn circuits are first energized.

To gain an elementary understand of this phenomenon consider the structure pictured in Figure 3. When a positive voltage is applied between anode and cathode of the device, junction J1 and J3 become forward biased whereas J2 is reverse biased. The center junction acts as a nonlinear capacitor which for an abrupt junction would have a capacitance of

$$C = \frac{K}{\sqrt{V + V_o}} \tag{5}$$

where V is the applied voltage, V_O the built in voltage of the junction and K a constant. To charge this capacitance current must flow through junctions J1 and J3. Current flow through the two end junctions result in minority carrier injection into the base regions of the device. If the charge injected is of sufficient magnitude and of a duration comparable to or shorter than the minority carrier lifetime the emitter efficiencies of the two junctions will rise. Since the pnpn will trigger into the conducting state when the sum of its alphas is unity, ⁸ i.e. when the equation

$$I = \frac{I_s}{1 - \gamma_1 \beta_1 - \gamma_2 \beta_2}$$
 (6)

tends toward infinity as a result of the rising emitter efficiencies of Junction J1 and J3. α_m is the emitter efficiency and β_m the transport factor for junction m, and I_s is the saturation current for junction J_2 , and α = $\gamma\beta$.

A practical solution to the rise in emitter efficiency with increasing current is the use of a "shorted emitter" as shown in Figure 4.9 Calculation of emitter shorts is described in section 3.1.2.3. At low current densities the current required to charge junction J2 will by-pass junction J3 so that the effective emitter efficiency is essentially zero. At higher current levels the lateral voltage drop in the base of the device will be sufficient so that current will choose to flow through the junction resulting in minority carrier injection in regions that are remote from the shorted area. This structure effetively solves the dv/dt problem in most applications. However, it does reduce the effective emitter area thus necessitating a larger silicon wafer or higher dissipation.

3.1.1.4 Turn-off Time

Turn-off time is determined principally by the minority carrier lifetime within the device. In addition the rate of rise of re-applied forward voltage following the recovery phase also affects the turn-off time.

The turn-off time or recovery time problem is one inherent with all minority carrier devices. In the case of a pnpn device it means that if the device is in the conducting state and the applied voltage is removed or reversed, a period of time called the turn-off time must elapse before forward voltage can be reapplied without having the device return to the conducting state. 10,11

The recovery time process can be visualized by considering the following simple model. Let the emitter efficiency of all the junctions be unity. By this we assume that when a forward bias is imposed across a junction it injects minority carriers into the lower impurity region but not the

higher impurity region. For our case holes would be injected across portion J1 into the n-type base and essentially no electrons into the p-type emitter; J2 would inject holes into its adjacent n-type base, but negligible electrons into the p-type base; J3 would inject electrons into its adjacent p-type base, but very few holes into the n-type emitter. Immediately following a period of forward conduction both base regions are saturated with excess carriers having a distribution as shown in Figure 4. With reversal of the applied voltage, current flow through the device is reversed and we have a net flow of charge out of each region proportional to current. In each base region the numbers of excess holes and electrons (i.e., above equilibrium values) are essentially equal. Thus, when the voltage is reversed those minority carriers in the immediate vicinity of the end junctions are swept out of the bases and the two end junctions become reverse biased as shown in Figure 5. However, as holes are swept out of base region n, they leave behind excess electrons which tend to lower the potential of n₁ with respect to p₂, thus forward biasing J2 so that it injects holes from p, to n,. As a consequence, holes leave base region n_1 on one side and are injected into it on the other side. In diffusing across the base, holes recombine with electrons at a rate proportional to minority carrier lifetime so that the quantity of excess electrons and holes in the base layer decreases exponentially with time. Since the current flow through the device is proportional to the excess charge in the base regions, the current decreases as the charge decreases. Thus for the case in consideration, the current is determined by the minority carrier lifetime of the device and decays exponentially with time according to the relation

$$I = K_1 + K_2 \exp(-t/\tau)$$
 (7)

where K_1 and K_2 are constants and τ is the minority carrier lifetime. To decrease the decay time the carrier lifetime must be lowered. This is being achieved by diffusing gold into the base regions. However, lifetime reduction must be carefully controlled because too much reduction will cause the forward conducting drop and the gate current required for

triggering to increase severely. A compromise can be achieved by reducing the base widths of the device as lifetime is decreased, thus maintaining good forward and triggering characteristics; unfortunately, the maximum blocking voltage attainable is also limited as a consequence. It appears that both devices B and C are very near to that theoretically achievable if full forward voltage is to be reapplied at the specified dv/dt level immediately following the recovery. Since many inverter applications require this type of operation, an attempt is being made to satisfy these much more severe conditions instead of those specified in MIL-S-19500/204.

3.1.2 Design Fabrication and Optimization

3.1.2.1 Introduction

As initially outlined, the program was to modify and improve the structure and the process used in fabricating the 2N1916W rectifier in order to meet the requirements of "Device B". "Device C" was to be a complete re-design, utilizing new processes on a radically different structural design.

Turn-off time has proven to be the most serious limitation in realizing reasonable yield processes. To meet all the requirements except turn-off time is in itself quite a problem but not as critical. However, as the minority carrier lifetimes of an SCR are reduced to lower turn-off time, the accompanying rise in forward drop causes the internal heat generation to rise. The problem can be solved by optimization of all the other design variables such as surface concentration, junction uniformity, surface contours, base resistivities and widths. However, such tight tolerances are required on each parameter that a very low yield is the result if the modified process of the 2N1916W is used. Consequently, it was decided that instead of continuing work with the alloy-diffused process for "Device B" and the all-diffused process for "Device C", the requirements of both devices

could best be met by combining the two programs and making both devices by the same process; i.e., by the all-diffused process.

Because both turn-off time and dv/dt effects play such a significant role in the design of both "Device B" and "C", much of the work during this past quarter has been directed toward optimizing and analyzing lifetime, and the shorted emitter.

3.1.2.2 Lifetime Effects

3.1.2.2.1 Basic Effects of Lifetime

The device characteristics which are affected by lifetime are as follows:

- 1) Reverse Blocking Current
- 2) Forward Blocking Current
- 3) Gate Current to Fire
- 4) Gate Voltage to Fire
- 5) Holding Current
- 6) dv/dt
- 7) Turn-on Time
- 8) Turn-off Time
- 9) Forward Voltage Drop

These are the characteristics which shall be analyzed here; but before doing this, let us summarize the basic effects of lifetime (recombination) in a semiconductor device. Carrier lifetime is lowered by the introduction of additional recombination centers by diffusing gold or some other lifetime killer into the silicon.

Recombination has the effect of either limiting the build-up of excess charge or causing the decay of excess charge in the bases. Recombination also partially determines the magnitude of diffusion current and together with the base width also determines the transport factor of the base. 12,13 C. T. Sah et al, 14 have shown that recombination in the space charge layer of a forward biased junction at low

current densities limits the emitter efficiency of the junction. The emitter efficiency, γ , of a junction is limited by recombination in another way since

$$\Upsilon = \frac{\int_{0}^{W_{E}} P_{p} dx}{\int_{0}^{W_{E}} P_{p}dx + \int_{0}^{W_{B}} N_{N}dx}$$
(8)

for a P-type emitter, where W_E and W_B are the emitter and base widths, respectively. However, if the diffusion length, L, for minority carriers is less than W_E or W_B , then the appropriate integral is taken over the diffusion length. Thus, if the limit of $L \rightarrow 0$, $\gamma \longrightarrow 1/2$ regardless of the impurity distributions in the emitter and base. Note that the above equation determines the maximum value of γ for a given impurity distribution.

Now with these considerations in mind, let us analyze the effect of lifetime on the above device characteristics assuming that all other device parameters (resistivity, geometry, etc.) are held constant.

3.1.2.2.2 Reverse Blocking Current

The reverse blocking current which flows through an SCR at voltages low enough so that "punch through" and "avalanche" effects need not be considered is affected by lifetime (recombination) by the following mechanisms:

1) Minority carrier diffusion in the bases towards the reverse biased junction J_1 and J_3 (see Figure 6). This current component is proportional to the reciprocal of the square root of the minority carrier lifetime; 12 i.e., proportional to $\frac{1}{L}$ where $L = \sqrt{D \tau}$ and L is the minority carrier diffusion length. Lowered lifetime increases this current component.

- 2) The component of current due to transistor action is determined by the current gain, $\alpha = \gamma \beta$, where γ is the emitter efficiency of J_2 in this case and β is the transport factor of the base in question. It is easily shown that $\beta = \operatorname{sech} \frac{W}{L}$ and therefore lowered lifetime decreases this current component. The lifetime dependence of γ is mainly that described by C. T. Sah et al; i.e., its variation with emitter current. The maximum value of γ is determined from impurity distributions.
- 3) A third component is due to generation of hole-electron pairs in the space charge regions of the reverse biased junctions J₁ and J₃. This causes a generation current as described by C. T. Sah et al. Lowered lifetime increases this current component.

At device junction temperatures of 125°C, all three effects are important.

3.1.2.2.3 Forward Blocking Current

The forward blocking current which flows through an SCR at voltages low enough so that "punch through" and "avalanche" effects need not be considered is affected by lifetime by the same mechanisms which apply to reverse blocking current; differing only with respect to the areas to which the mechanisms apply. The current components of these mechanisms are as follows:

 Minority carrier diffusion currents in the bases toward the reverse biased junction J₂ which are proportional to

$$\frac{1}{I_1} = \frac{1}{\sqrt{D_1}}$$

- 2) Transistor action current determined by the alphas of the transistors formed by J_1 and J_2 and by J_3 and J_2 .
- 3) Space charge generated current in the space charge region of \mathbf{J}_2 .

At operating temperatures of 125°C, effects 1) and 3) should be the most important. Transistor action is more important here than in the case of the device being reverse biased since the emitter efficiencies in this case are much higher.

3.1.2.2.4 Gate Current to Fire

The gate current to fire is measured by placing across the SCR an anode-to-cathode voltage which is half the rated voltage. A pure DC voltage is then applied to the gate. The voltage is increased until the device fires completely. The gate current to fire (I_{GT}) is then taken as the gate current corresponding to this voltage (V_{GT}).

In order to understand the turn-on mechanism of an SCR in terms of charge analysis, consider Figure 7, which gives the approximate minority carrier charge distributions for the "off" and "on" states of an SCR. Since one normally assumes charge neutrality to exist in the bases, we must also have an equal excess of majority carrier charge. In the "off" state, a small amount of excess charge exists in the bases since we have a small forward blocking current flowing through the device. In order for the SCR to switch to the "on" state, the bases must be saturated with a sufficient amount of charge so that J₂ becomes forward biased. The bases may be forced into saturation by any one of the following methods:

- 1) Application of a sufficiently large gate current. 16
- 2) Application of an anode to cathode voltage equal to or greater than the static ^V (BR)FO of the device, so that the avalanche multiplication effects can occur, ^{17,18} and
- Application of an anode to cathode voltage having a sufficiently large dv/dt.

At the moment, we are interested only in the case of gate turn-on. If space charge generated current is neglected, the forward blocking current which will flow through an SCR at forward voltages low enough so that avalanche may be neglected is given by 18

$$I = \frac{I_{CO}}{1 - \alpha_{NPN} - \alpha_{PNP}}$$

where I_{CO} is the leakage current through J_2 if J_2 is reverse biased and isolated from J_1 and J_3 . From this it can be seen that if $(\alpha_{NPN} + \alpha_{PNP}) \stackrel{\geq}{=} 1$, then the above equation is invalid and the device has switched to its on state. The current gain α , is a function of emitter current as shown in Figure 8. The SCR is constructed such that $(\alpha_{NPN} + \alpha_{PNP}) < 1$ for low current levels, but allows $(\alpha_{NPN} + \alpha_{PNP})$ to become greater than unity by the mechanism described by C. T. Sah et al, when a sufficient amount of gate current is applied.

F om the above comments one concludes that the effect of lifetime on gate current to fire is quite dependent on the effect of lifetime on α_{PNP} and α_{NPN} . In other words a decrease in the alphas will cause an increase in the gate current to fire. A decrease in lifetime will cause a decrease in $\alpha = \gamma \beta$ as follows:

- 1) The maximum value of the γ 's will change slightly.
- 2) The limiting effect of recombination in the space charge layers of J_1 and J_3 on the γ 's will increase.
- 3) The transport factor, β , will decrease.

3.1.2.2.5 Gate Voltage to Fire

The gate voltage, V_{GT} , to fire was defined in the previous section and the effects of lifetime on it will be the same as the effects of lifetime on gate current to fire, I_{GT} , since I_{GT} is proportional to e

3.1.2.2.6 Holding Current

The holding current of an SCR is defined as that forward conducting current below which the SCR reverts to its forward blocking state with the gate open. In terms of charge this means that just enough charge at some current level is being injected into the bases as is being recombined such that Junction J_2 just barely stays forward biased.

In terms of current, this means that the current level has fallen to the point at which $\alpha_{NPN}^{\alpha} + \alpha_{PNP}^{\alpha} = 1$. Since the holding current depends on α_{NPN}^{α} and α_{PNP}^{α} in the same way as does the gate current to fire, we would expect the same dependence of holding current and gate current to fire on lifetime; therefore, decreased lifetime increases the holding current.

3.1.2.2.7 dv/dt

The dv/dt capability is defined as the maximum rate of rise of forward voltage that the SCR will support without triggering.

Basically, dv/dt firing is the rapid charging of junction J₂ causing a release of charge into the bases, which with subsequent transistor action, results in device turn-on. This effect may be decreased by decreasing lifetime since this will cause:

- more recombination of charge in the bases and a subsequent decrease in the transport factors, and
- 2) more recombination in the space charge regions of J_1 and J_3 and thus decrease the emitter efficiencies of these junctions.

3.1.2.2.8 Turn-on Time (Gate commutated)

The turn-on time of an SCR is defined as the time interval between the initiation of the gate signal and the time when the resulting forward current reaches 90% of its final value while switching to the "on" state by gate firing.

Turn-on time is increased as lifetime is decreased. The relative effects of lifetimes on turn-on time are now being studied.

3.1.2.2.9 Turn-off Time

When turn-off time is measured under standard test conditions, the SCR is initially in an "on" state, then a small reverse bias is applied and finally a forward voltage is reapplied with a fixed rate of rise. The turn-off time is defined as the time measured from the point at which the reverse voltage is applied to that point at which the SCR starts to block the reapplied forward voltage.

In order to understand what this means in terms of the device, we must remember that when the device is in the "on" state the two bases of the SCR are "saturated"; i.e. contain enough excess charge to switch the center junction to a forward biased condition. While the device is in the reverse bias condition, most of this excess charge must be removed from the two bases, so that the device will block the reapplied forward voltage.

While the device is reverse biased the excess charge is removed from the bases by a number of ways, the most important of these are as follows:

- 1) When the device first sees the reverse voltage, J₁ and J₃ will collect a large number of minority carriers until J₁ and J₃ can support the reverse voltage after which the current passing through these junctions will be a decaying minority carrier current the magnitude of which is dependent upon the concentration and lifetime of minority carriers in their respective bases.
- 2) The excess charge is continuously recombining in the two bases at a rate which is dependent upon the concentration of excess minority carriers and their lifetime.
- 3) Majority carriers in the P-type base have an opportunity to leak out through the gate circuit. The magnitude of this current is, of course, dependent on the impedance of the gate circuit.
- 4) Since J₂ is forward biased, it acts as an injecting junction of minority carriers. Its injection efficiency is dependent to some extent upon base lifetime; however, it is, in general, quite high in the direction of injection from the P-type base to the N-type base.
- 5) Some recombination in the space charge layer of J₂ may occur, the magnitude of which depends on the current going through the device. This effect probably has a negligible effect on turn-off time.

Considering the above factors one sees that turn-off time is limited mainly by the inability of the N-type base to discharge itself quickly, since this discharge is controlled predominately by factors 1) and 2); that is, current flow through the device is determined by the minority carrier lifetime of the device. (See also section 3.1.1.4) The lower the lifetime, the faster the rates at which 1) and 2) occur and the faster the decay of the current flow.

3.1.2.2.10 Forward Voltage Drop

Forward voltage drop of an SCR is defined simply as the voltage drop from anode to cathode of the device in the "on" state. This includes lead and contact drop, of course, which we shall not consider, since they are not a function of lifetime. Inside of the device we have voltage drops across each of the three junctions and across each of the four regions shown in Figure 6. The voltage drops across the junctions should not be lifetime dependent since the limiting effect of recombination in the space charge layers is reduced significantly at the normal operating currents. Now we must remember that a field current has a voltage drop associated with it, while a diffusion current does not. Also, field current is not lifetime dependent while diffusion current is. The currents in the emitter regions are almost entirely field dependent so that there are voltage drops in these regions but they are not lifetime dependent. However, the currents in the bases are both field and diffusion currents. Now, if we take all our measurements of voltage drops at the same current level, which is only reasonable, the more recombination we have in the bases, the more field current we will have in the bases. Thus, as lifetime decreases, the voltage drop in the bases and also the total voltage drop of the device will increase.

3.1.2.2.11 Summary

In summary turn-off time can be decreased by lowering the carrier lifetime and maintaining the base widths at a minimum compatable with the voltage capacity required. Of the other transient properties dv/dt will be improved and turn-on time increased slightly. Other device characteristics such as blocking currents, gate triggering current and voltage, holding current and forward voltage drop will be increased but the increases will not be serious except in the case of forward voltage drop. An excessive increase in the forward voltage drop could hamper the current carrying capacity of the device.

Experiments are being conducted using gold diffusion to optimize the carrier lifetime for device characteristics. Gold diffusion temperatures between 800°C and 900°C are being used. A curve of lifetime as a function of gold diffusion temperature from the Bell System Technical Journal (January 1960) is shown in Figure 9.

3.1.2.3 Calculation of Emitter Shorts (See also section 3.1.1.3)

The purpose of an emitter short is to prevent significant injection of minority carriers by the PN junction in the neighborhood of the short at low current levels. As this low level current increases it approaches the forward current necessary to turn-on the SCR.

The value of the current necessary to turn-on the SCR should be greater than the displacement current of the SCR under the highest expected dv/dt conditions. Calculation of the amount of shorting needed is dependent, therefore, upon the emitter characteristics at the temperature under consideration, and the displacement current.

Perhaps the place to start is to determine what is a significant injection of minority carriers. It will be assumed that steady state emitter junction characteristics apply. Figure 10a shows the familiar alpha vs. current curve for a junction transistor. The current at point p where $\alpha_1 + \alpha_2 = 1$ will just turn-on an SCR.

When the emitter is partially shorted as shown in Figure 10b, the total forward current necessary to turn-on the SCR increases from p'toq'. (Note that the combined characteristic at much higher current levels has not been altered by the presence of a short.) This higher forward current necessary to turn-on the SCR means larger allowable displacement currents and higher allowable dv/dt ratings for the SCR.

For small area SCR's where transverse resistance in the base layers is negligible, the short can be placed between cathode and gate, internal or external to the package. The conductance of this short could be

$$Y = \frac{I_{q'} - I_{p'}}{V_{p'}}$$
 (10)

where I_q , is the displacement current C dv/dt, I_p , is the junction current which is assumed equal to $I_o = \begin{bmatrix} \frac{q \left(V_D - V_{app} \right)}{kT} \\ e \end{bmatrix}, (1 \le 7 \le 2),$

where V_D is the built-in voltage and V_{app} is the applied voltage, and V_p , is the voltage across the emitter junction. C is the barrier capacitance of the middle junction. Substitution gives

$$Y = \frac{C \frac{dv}{dt} - I_{p'}}{V_{D} - \frac{7kT}{q'} \ln (1 + I_{p'})}$$
(11)

The usual voltage reapplied across an SCR has a dv/dt that decreases as the voltage increases. The barrier capacitance C also decreases as the voltage across the SCR increases. The value of $\mathbf{I}_{p'}$ decreases at the voltage increases because of the narrowing of the base widths. Furthermore, the temperature dependence of the $\mathbf{V}_{\mathbf{D}}$, $\mathbf{I}_{p'}$, $\mathbf{I}_{\mathbf{O}}$ is very strong. I also varies rapidly with minority lifetime. For these reasons, an exact solution giving the necessary short conductance is not easily obtainable even for the case of negligible cross-biasing

in the base. Once Y is obtained its temperature dependence will likely differ from that of the short conductivity. Any practical determination of short conductivity will, therefore, be based upon a number of judicious assumptions. For large area devices like "Device B" or "Device C" the effectiveness of emitter shorts is also dependent upon the transverse field in the base layer. This relationship is not too difficult to determine analytically. Therefore the design of a shorted emitter will be based upon this calculation plus reasonable assumptions made about the junction characteristics discussed above.

Assumptions (Refer to Figure 11)

- a) The displacement current enters the base layer uniformly across the base area.
- b) All the displacement current leaves the base layer via the short path.
- c) The base layer is extremely thin compared to its diameter so that it can be :haracterized by a sheet conductivity, σ s.
- d) Negligible injection occurs when the voltage across the PN emitter junction is less than Ve.

Solution

The voltage drop between points b and a, (V_{ba}) in Figure 11, must be less than Ve to keep the SCR from turning on by a rapid rise in anode voltage. Using cylindrical coordinates this voltage drop is

$$V_{ba} = R \frac{J_D}{\sigma s}$$
 (12)

Where R is the geometry factor

$$R = \frac{1}{16} \left\{ d^2 + D^2 \left[2 \ln \left(\frac{D}{d} \right) - 1 \right] \right\}$$
 (13)

and $J_{\overline{D}}$ is the displacement current

$$J_{D} = C \frac{dv}{dt}$$
 (14)

Solving Equation (13) for R and substituting

$$R = \frac{\sigma s \ Ve}{C \frac{dv}{dt}} \tag{15}$$

The value for σ s can be calculated from a knowledge of the diffusion profiles. Reasonable values of Ve and C are 0.5 volts and 800 pf/cm² respectively. Equations (13) and (15) define a relationship between d and D which satisfy the above conditions for any particular value of dv/dt. The output from a calculation of this type performed on a General Electric model 225 Computer is shown in Figure 12. This output was calculated for "Device C" and shows the required short dimensions. It is interesting to note that the percentage of contact area used by the shorts reduces as the dimensions of the short becomes less. There is a practical limit, however, to the smallest size of short that can be made.

3.1.3 Rating, Testing and Characterization

Both device B and C are being tested and rated according to the criteria and methods listed in the following sections. Parameters for Device B will be used as examples. The symbols used are shown in Appendix A, PART III.

3.1.3.1 Voltage (V ROM, V ROM, and V)

The SCR's are characterized at 25°C and 125°C for voltage blocking ability by applying a half sine wave, forward or reverse voltage, and monitoring current by means of an E-I trace on an oscilloscope. The voltage is increased until one of the following events occur:

- Break over The device goes into the "on" state in the forward direction.
- 2) Break down The device avalanches.
- 3) Blocking current reaches a predetermined value (10 ma)
- 4) Erratic E-I trace (reject).

The lowest of the four voltages (V_{ROM} at 25°C, V_{FOM} at 25°C, V_{ROM} at 125°C and V_{FOM} at 125°C) determines the test or classification voltage. In order to be classified a 1000 volt unit, the lowest of the four voltages must be at least 1,100 volts. Blocking currents are remeasured at the maximum

operating junction temperature and classification voltage (V_c). They must be significantly lower than that required to cause thermal runaway. A pictorial representation of the blocking characteristic is shown in Figure 13.

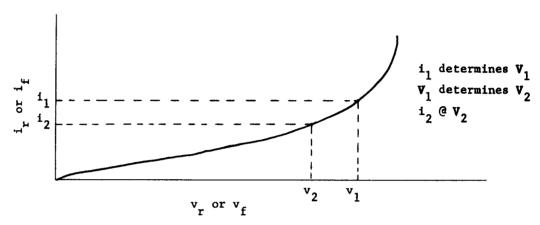


Figure 13 - Blocking characteristic

3.1.3.2 Current Carrying Capability (I at Tc)

The maximum average current a device can carry is determined by the maximum permissable peak junction temperature, the power dissipation within the device (total losses), and the heat dissipation capability (transient and steady state).

A computer rating program is being used to determine the maximum limits of effective thermal resistance and conduction losses so that T_J will never exceed 125°C when $T_O = 70$ amperes at $T_C = 90$ °C.

- a) The maximum permissible junction temperature was set at 125°C which is the generally accepted maximum operating temperature for SCR's. All high temperature testing was done at this point.
- b) Power dissipation within the device is composed of the following components:
 - (1) Gate Power

 The average gate power is determined by the maximum gate voltage and current (V_{CF} and I_{CF}).

(2) Blocking Losses

The average blocking losses are determined from the blocking current limits.

(3) Conduction Losses

The on-voltages were measured on a number of units at current levels from 1 amp to destruction at 25°C and 125°C. All units must have on-voltages less than the maximum curve as determined by the computer calculations.

- (a) Low current level on-voltage at 25°C (refer to E50 GX-15-S1 included in PART III). The 1 ampere V_f is obtained by first firing the device into a high current (approximately 50 amperes), by reducing the current without interruption to 1 ampere DC and by reading the DC voltage across the unit.
- (b) High current level on-voltage (forward drop) at 25°C (E50 GX-14-S1, PART III). A 2 m sec half sine wave current pulse of 500 amperes peak is passed through the device; the on-voltage is displayed on an oscilloscope.
- c) Heat dissipation ability
 - (1) Thermal Resistance

A number of devices are tested for transient thermal impedance per E50 GX-30-S1 (PART III), and the maximum reading of all these devices is used as the maximum transient thermal impedance.

(2) All devices are tested for Effective Thermal Resistance per E50 GX-28-S1 (PART III). Units which fail to meet the maximum thermal resistance as determined by the computer program are rejected.

3.1.3.3 Speed

Three speed characteristics; turn-on time, turn-off time, and dv/dt are measured as described in the following paragraphs.

3.1.3.3.1 Turn-on Time at 25°C

The circuit shown in Figure 14 is used to measure the turn-on time (t_{on}). The SCR is triggered-on at a peak voltage of approximately 6 volts. The gate current is monitored with a confent probe and amplifier to insure that it does not exceed 80 ma. The gate voltage and the load current are displayed on an oscilloscope to measure the turn-on time; this is the time from when the gate voltage reaches 50% of the final value to when the resultant current through the device rises to 90% of final value.

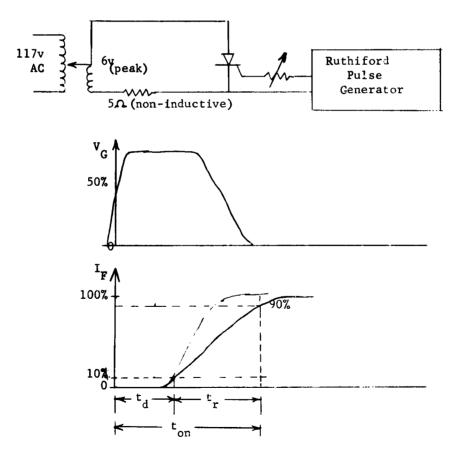
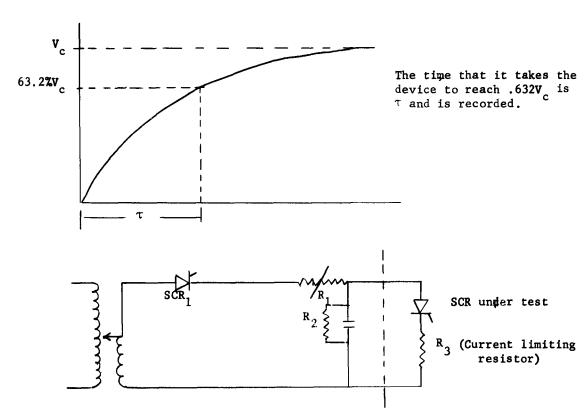


Figure 14 - Turn-on time weasurement

3.1.3.3.2 dv/dt (Rate of Rise Test)

The circuit shown below is used to dermine the maximum rate of rise of forward blocking voltage the device can withstand.

The device is placed in a heated block at $125\,^{\circ}\text{C}$. The voltage is increased until the peak voltage across the SCR under test is the Rated Voltage. SCR₁ is triggered at the peak of the line voltage. The voltage across the capacitor and SCR under test exponentially increases with a time constant of R₁ C₁. The voltage across the SCR under test is viewed with an oscilloscope. R₁ C₁ is decreased until the device switches into the on-state; R₁ C₁, is then increased until the SCR can regain blocking ability.



3.1.3.3.3 Turn-off Time

With the device in a heat sink at 125°C, the current and voltage shapes shown in Figure 15 below are generated.

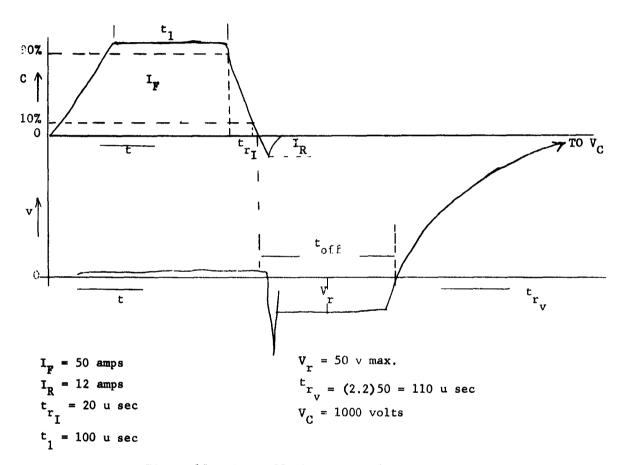


Figure 15 - Turn-off time generation

Turn-off time is the time between the current crossing down through zero, and voltage crossing up through zero.

These shapes are generated by the circuit shown below in Figure 16.

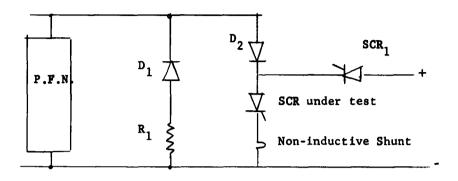


Figure 16 = Turn-off time test circuit

When the SCR being tested is triggered, the pulse forming network discharges through \mathbf{D}_2 , the SCR under test, and the current shunt. The current reversal goes through the parallel paths \mathbf{D}_1 , \mathbf{R}_1 , \mathbf{D}_2 , and the SCR under test, and the shunt. When either \mathbf{D}_1 or SCR₁ recovers reverse blocking ability, all reverse current goes through \mathbf{R}_1 and \mathbf{D}_1 .

The voltage drop across D_1 and R_1 is applied in the reverse direction across D_2 and SCR_1 . The recovery times of D_2 and the SCR under test must be reasonably well matched in order to measure $t_{\rm off}$ accurately.

At some time after the SCR being tested has triggered, SCR₁ is fired applying an exponentially increasing voltage across the SCR under test. This time is decreased until the SCR under test can not block this forward voltage, then increased until it regains blocking ability. This latter time is the measured turn-off time.

3.1.3.4 Other Characteristics

3.1.3,4.1 Holding Current

 $I_{\rm H}$, the holding current is measured at 25°C and 125°C using the circuit shown in Figure 17. The unit is initally fired into a load of 500 ma DC.

PART II

4.1 Program for the Next Quarter

Optimization of design parameters will continue with increased emphasis on turn-off time and forward conducting drop. Final design samples of Device B will be constructed, evaluated and delivered. Fabrication and evaluation of the final design devices will be the primary goal for the next quarter.

Theoretical work on Device C will be continued.

APPENDIX A

PNPN TYPE SWITCH LETTER SYMBOLS

1. Abbreviations

Quantity Symbols

Current I, i
Voltage V, v

Power P, p

Thermal Resistance 9

Time t (lower-case only)

Temperature T (upper-case only)

Subscripts

Anode A, a

Cathode K, k

Gate G, g

Forward F, f

Reverse R, r

Maximum Value M

Average Value (AV)

2. Convention to be Used Where "*" is Shown (See Table):

- 0, 0 Gate terminal is open-circuited or device has no gate terminal.
- S, s Gate terminal is short-circuited to the terminal of the adjacent region.
- X, x Gate terminal is returned to the terminal of the adjacent region through a stated impedance and/or bias voltage.

3. Specific Letter Symbols

NO	NOTE: *	means additional (See	subscript must be used here. Section 2)	used here.	
Quantity	Total RMS Value	DC Value, No Alternating Component	DC Value, With Alternating Component	Instantaneous Total Value	Maximum (Peak) Total Value
Forward Current, on State	J	I	^T F(AV)	1.	Мď
Forward Current, On State 180° conduction angle, 60 c.p.s., Half Sine Wave Current		_	01	:1	l
Repetitive Peak Forward Current	_		-	1	IFH (rep)
Peak Surge Forward Current	-	-	_	1	LFM (surge)
Forward Breakover Current	-	I (BR)F*	_	¹ (BR)F*	-
Forward Blocking Current	* ^J I	^z ¥ ₁	[F*(ΑV)	¹ P*	Жа́Т
Reverse Blocking Current	Ir*	I _R *	^T R*(AV)	1 R*	I _{R*M}
Reverse Breakdown Current	1	I (BR)R*	1	1 (BR)R*	l
On Voltage	Vf	V _F	^V F(AV)	ă'n	VFM
Forward Breakover Voltage	ı	V (BR)F*	+	V(BR)F*	-
Forward Blocking Voltage	V _{f*}	V _F *	V _{F*} (AV)	*4 _^	й*ā _л

3. Specific Letter Symbols (Contt)

Quantity	Total RMS Value	DC Value, No Alternating Component	DC Value, With Alternating Component	Instantaneous Total Value	Maximum (Peak) Total Value
Reverse Blocking Voltage	*1 V	V _R *	V _{R*} (AV)	[∨] R*	V _{R*M}
Working Peak Reverse Blocking Voltage	i	-	-	-	V _{R*M} (wkg)
Repetitive Peak Reverse Blocking Voltage	l	-	_	-	V _{R*M} (rep)
Non-Repetitive Peak Reverse Blocking Voltage	l	1	_	9	V _{R*M} (non-rep)
Reverse Breakdown Voltage	ţ	V(BR)R*	-	V (BR)R*	-
Holding Current	1	H	*	H,	l
Gate Trigger Current	l	$^{ m I}_{ m GT}$	_	$^{1}{ m cr}$	LGIM
Gate Turn-off Current	-	T _{GQ}		ბ9 _‡	ЖÒÐ
Forward Gate Current	$^{\mathrm{I}}_{8^{\mathrm{f}}}$	$\mathbf{I}_{\mathbf{GF}}$	^I GF (AV)	$^{1}_{\mathrm{GF}}$	IGFM
Reverse Gate Current	ıgı	LGR	IGR (AV)	1.GR	LGRM
Gate Trigger Voltage	_	V _{GT}	-	TD ^v	V _{GTM}
Gate Turn-off Voltage	ı	VGQ	1	v 60	У СОМ
Forward Gate Voltage	$^{V}_{8f}$	VGF	^V GF (AV)	aD _∧	лед
Reverse Gate Voltage	Vgr	A.S.	^V GR (AV)	85 ^	VGRM
Gate Power Dissipation	ı	PG	P _G (AV)	P _G	P.GM

Ambient temperature	T _A
Case temperature	T _C
Junction temperature	$\mathbf{T_{J}}$
Storage temperature	$\mathtt{T}_{\mathtt{stg}}$
Thermal Resistance	θ
Thermal Resistance, Junction to Ambient	θ _{J-A}
Thermal Resistance, Junction to Case	θ _{J-C}
Transient Thermal Impedance	θ.,
Transient Thermal Impedance, Junction to Ambient	θ(t) θ _{J-A(t)}
Transient Thermal Impedance, Junction to Case	-A(t) θ _{J-C(t)}
Delay Time	^t d
Rise Time	t _r
Fall Time	t _f
Storage Time	t s
Pulse Time	t _p
Turn-On Time, Gate Commutated $(t_d + t_r)$	^t G on

Turn-Off Time, Circuit Commutated $\begin{array}{c} t_{off} \\ \\ \text{Rate of Rise of Forward Blocking Voltage} \\ \\ \hline \\ \frac{d \left(v_{F0} \right)}{dt} \\ \\ \text{Peak Reverse Surge Power} \\ \\ \text{Applied Anode - to - Cathode Voltage} \\ \\ \text{Classification Voltage} \\ \\ \text{Diffusion Voltage (Built-in Voltage)} \\ \end{array}$

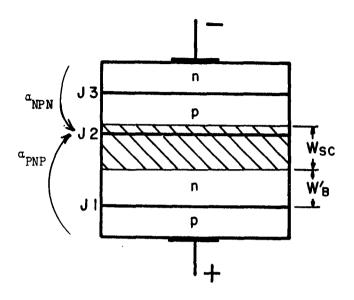


Figure la - Space charge layer resulting from forward blocking voltage

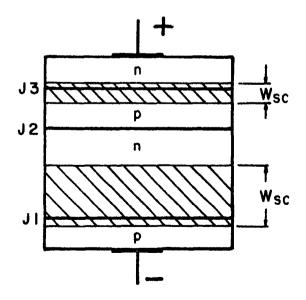


Figure 1b - Space charge layer resulting from reverse blocking voltage

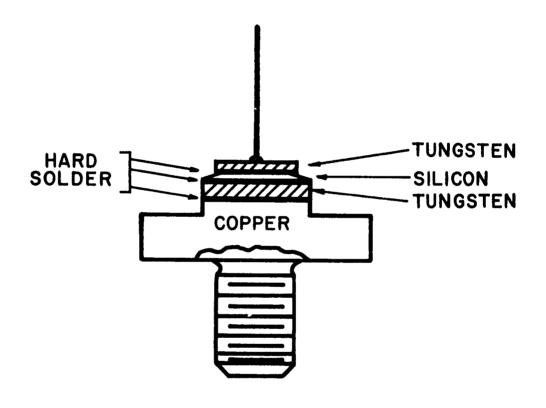
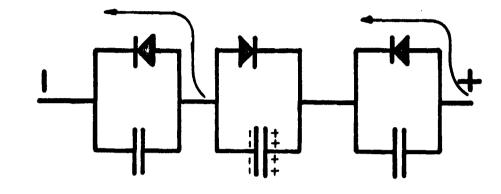


Figure 2 - Silicon device utilizing transition plates and hard solder



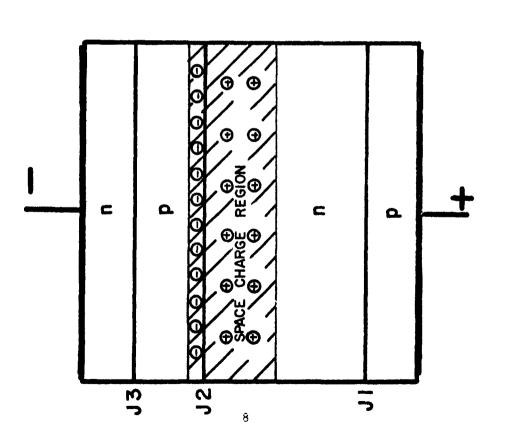


Figure 3 - Space charge layer visualized as capacitance which must be charged through emitting cathode and anode junctions

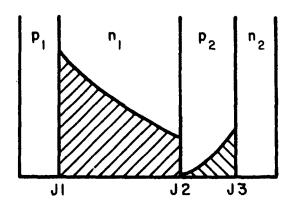


Figure 4 - Excess hole and electron distribution in base regions during forward current flow

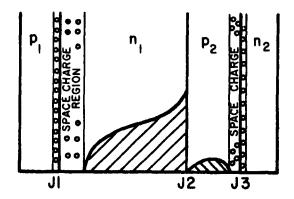


Figure 5 - Hole and electron distribution during recovery current phase

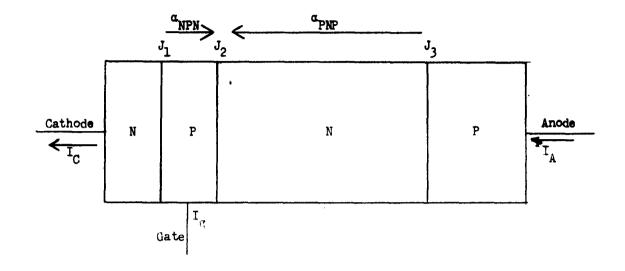


Figure 6 - Schematic diagram of an SCR

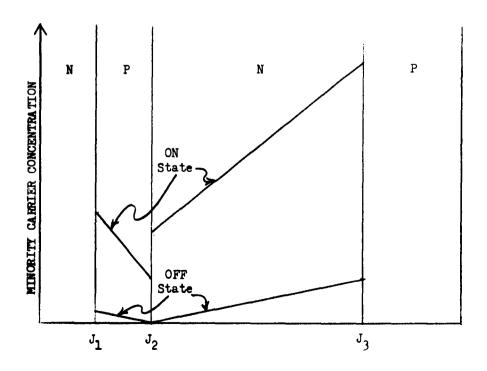


Figure 7 - Minority carrier distributions 10

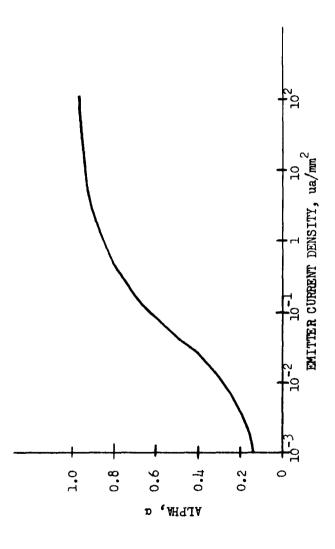


Figure 8 - Alpha as a function of emitter current

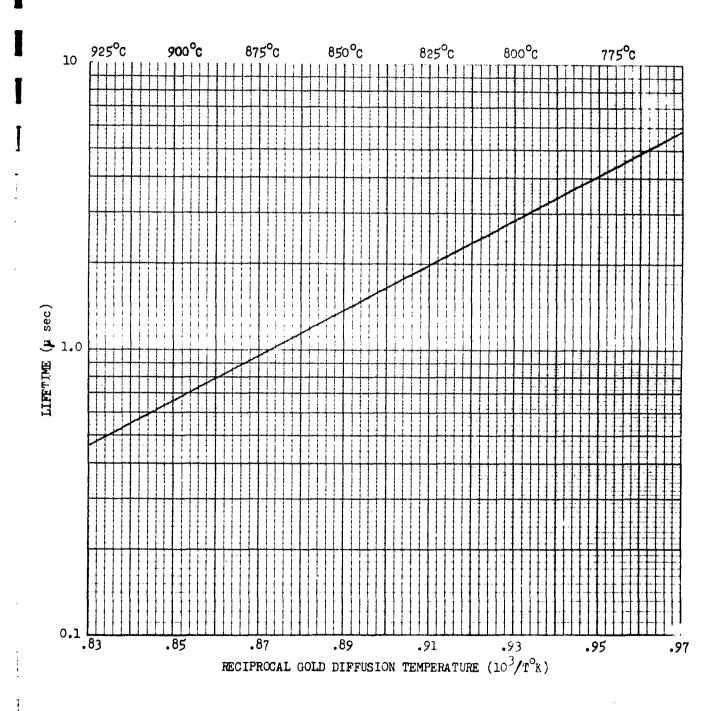


Figure 9 - Lifetime in silicon as a function of gold diffusion temperature

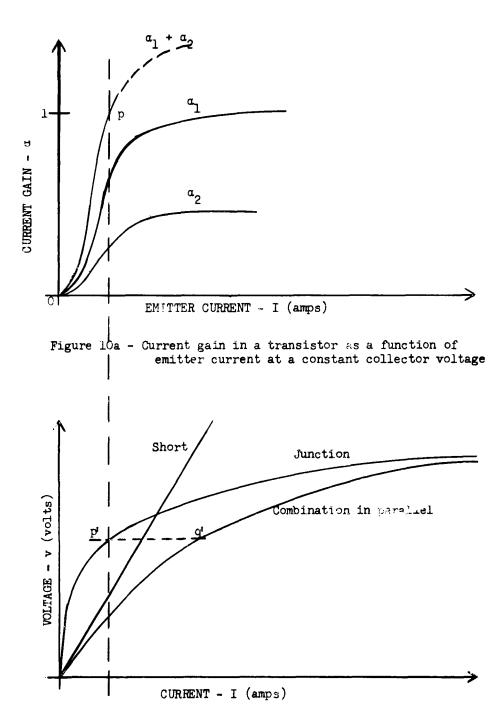


Figure 10b - E-I characteristics of an emitter that has an ohmic short

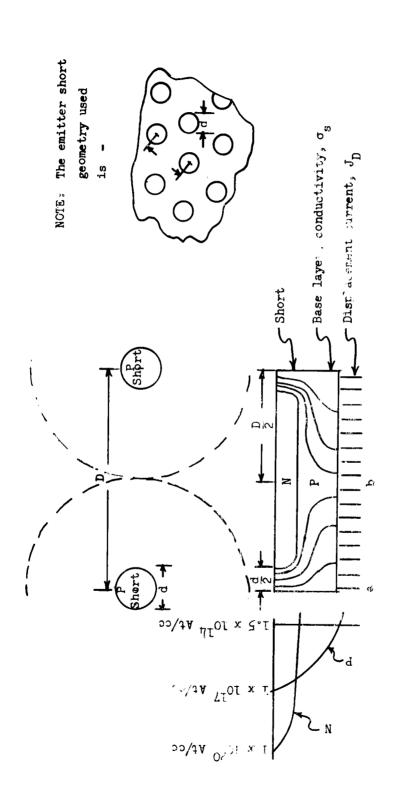


Figure 11 - The emitter short

Militare (and prompting and an also (also as	SH	ORTED	EMITTER	GEOME	rry	
INPUT DATA						and the state of t
SURFACE CONC	RASE C	ONC	JUNCTION	DEPTH	TREGION	
.09999999	18 .149	99994 15	.76199	999 -2	.50799999	-2
DVDT	CAPAC	TACE	VOLTAGE	DROP	AVE-COND.	
.20000000	9 .799	99828 -9	.49	999952	.05440262	1
OUTPUT FOR T	RIANGULAR	DOT SHO	PRTS			
	RIANGULAR			OF SH	ORTS	
				OF SH	ORTS	
				OF SH	DRTS	
	RT DIAM.	SPACING 92 107			DRTS	
	RT DIAM.	92 107 123		.042	ORTS	
	20 30 40 50	92 107 123 139		.042 .070 .095	ORTS	
	20 30 40 50	92 107 123 139		.042 .070 .095 .116	ORTS	
	20 30 40 50 60	92 107 123 139 153 162		.042 .070 .095 .116 .138	ORTS	
	20 30 40 50	92 107 123 139		.042 .070 .095 .116	ORTS	

Figure 12 - Computer data for shorted emitter geometry

P P Ty = 125°C ± 3° toff Tapp I G NOT MEASURED H S ×50 \$ • Ty = 25°C ± 3° g 80. .952.08 .092.83 .81 **№** 9 .052.4 .202.6 .0dt.9 **,** € PG (E) 12 P T, - 125°C ± 3° (BR)FO or FO (BR)BC or 1,000 (BR) NO. 42 1.5 53 1.3 48 1.4 26 1.0 47 1.7 40 1.0 25 0.9 Į, (m) 2 2 2 2 2 2 2 2 6 2 2 T. - 25c . 3' (BR)FO or 70 1.5 (E) (E) (E) 2 2 800 E-75 OR 10 P 11 12 13 14 AH STUD

g Š

Date 30 April 1963

DEVICE B DATA SHEET

<u> </u>	B-76					-		DEVICE	m	DATA SHEET						9 5	30 Ap	30 April 1963	963		
- 41		eH T	1, - 25c + 3 ^c	,				T.	125°C ±	30			ائ <u>ا</u> ا	Ty = 25°C ± 3°			T.	- 125°C ± 3°	30		
१ ३४५०	Off and	1(BR)EO or 1EO	(BR)FO or PPO	1(BR)FO or 1 _{FO}	j5	er er	*(BR)BO or *BO	1(BR)RC or 1RO	(BR)FO or FPO	¹ (BR)PO or ¹ PO	Ţ		$\begin{pmatrix} \mathbf{V}_{\overline{\mathbf{F}}} & \mathbf{V}_{\overline{\mathbf{F}}} \\ \mathbf{A} \end{pmatrix}$ (a)	re o	Œı	T _{ED}	toes / *4pp		4(vp) /	/ *app	
-	940	10	096	10	37	1.0	860	01	790	12	10	9.0	.186.	∞	26		17 7	700	100	909	
7	920	10	096	20	30	1.0	860	10	820	25	11	0.61.0	.0 2.2	5.2	24		13 8	800	125	700	
က	710	10	700	50	,		630	10	340	20	,	,	.791.9	9.8	21		<u> </u>		285	200	
4	> 1000	10	920	0+	<u> </u>	<u>/\</u>	>1000	10	079	20	1	<u></u>	.2 2.3	15.0	41		10 6	009	250	200	
47	096	01	860	40	22	1.0	860	10	009	20	10	0.6	.0 2.2	7.2	32		14 600	00	170	200	
9	800	10	840	25	,		240	10	800	1.5	,	,	.9 2.2	•	22		17 7	700	170	200	
7	910	10	780	50	21	0.8	840	10	520	25	10	0.61	.0 2.5	7.0	21		10 5	200	170	200	
œ	>1000	10	860	45	22	6.0	920	10	650	30	10	0.41.0	.0 2.6	8.0	27	ED	10 6	009	200	009	
6	880	10	910	25	59	1.5	800	10	820	15	23	1.0	- 2.1	23.0	41	SUR	13 8	800	140	009	
10	780	10	840	55	25	8.0	740	10	790	30	11	9.0	.8 2.0	7.0	20	MEA			185	500	
11	200	10	066	8	1	,	440	10	820	25	,	1	.3 2.6	10.8	35	Ţ	80	800	250	800	
12	920	10	940	25	25	6.0	850	10	700	10	12	0.6	.0 2.5	7.0	*	ON	12 6	009	200	009	
13	880	10	006	40	70	0.9	700	10	760	25	6	9.0	.9 2.3	9.9	21		17 7	700	23	200	
ä	: (6) 1 (7)	- 3 aspers - 500 aspers				1		1	TABLE 3]]	1	

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		dd*_/	009	200	200	1	400	900	700	800	400	400	
1963	- 125°C + 3°	/ (^{QL}) /	30	25	25	,	∞	360	350	36	∞	10	
30 April 1963	, = 125°	ad ·	009	200	200	800	400	006	700	800	400	400	
30 A	1,	dde_/JJ03	18	19	30	6	2	9	7	20	20	8	
Date		0E ₁				(BED	us v:	WE	T	ON		
		QI ₁	15	21				1	•	15	11	•	
	25°C ± 3°	to on	2	6	•	•	•	•	16	4	ı	ო	
	T, 25	رق (ق)	.85	<u>-</u>	2.6	1	1	ょ	5.0	3.2	2 . 45	1.85	
:		₽ 84 €	366.	1.1	1.0	•	2.6	2.3	1.11.63	1.0	.97 2 .45	.76 1.85	
		4 G7	•	0.5	1		1.1	1.1	1.1	9.0	1	,	
,		خل	'	ъ	•	,	42	35	28	5	ı	,	
DATA SHEET		1(BR)FO or 1FO	7.5	89	10.	10.	25.	15.	22.	12.	10.	20.	
B DATA	Ty = 125°C ± 3°	(BR)?0 or *P0	720	099	620	980	1050	830	1080	006	979	650	TABLE 4
DEVICE _	£3	1 (BR) RC or 1 RO	10	10	10	10	25	10	24	15	10	10	ā
		*(BB)BO or BO	820	860	099	066	1050	700	1140	1065	880	800	
		V GT	8.0	8.0	,	,	1.3	1.2	1.4	0.8	,	,	
		Let	6	13	,	,	2	41	59	10	,	1	
	,	¹ (BR)PO or ¹ PO	10	6	20	20	10	20	01	12	20	10	
	T, = 25°C = 3°	(BR)FO or FO	1260	1100	066	1050	1080	1070	1095	1200	1150	1290	į
	H.	OH (HE)	10	10	10	,	10	7	-	10	10	10	1, - 1 aspere 1, - 500 esperes
E-77		(BR)RO or N	1300	1150	920	1190	1080	1140	1230	1350	1140	930	 @
ist 16.	-41	स ३५५०	-	2	٣	4	2	9	7	∞	6	10	 : SEC

The parameter The paramet	4 5	E-78		1					DEVICE'B"		DATA SHEET					Ħ) te	O Ap	Date 30 April 1963	963	V
Challes * Challes				1 = 25°C ± 3°					T,	• 125°C ±	٠,٠		\vdash	, , , , , , , , , , , , , , , , , , ,	1 +4			4.7	2521 •	* 3°	
120 10. 120 1.0		(BR)RO or		(BR)FO	1	Į.		(BR) RO or	1(BR)RC or 1RO	*(BR)FO or *FO	1(BR)FO or 1 _{FO}				on O	¹ B		, oce / v		(4th)	4bb
1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1,	4-	1220	2	1230	7.0	76	1.2	740	10.	1260	7.5	-	-	l	13.	47	2			1233	740
1470 0.1 1200 1.0. 46 1.0 1260 7.5 1220 10 88 2.7 - >50 17 1000 - 1 14.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1		1690	10	1220	1.5	32	1.0	1240	&	1180	5.				∞	25	<u>_</u>			1000	400
1470 0.1 1290 3. 18 0.8 1290 10. 1245 10. 5 0.6 .8 1.2 4 22 40 1000 46. 1440 0.2 1350 4. 73 1.26 10. 1320 10. 1320 10. 23 1.0 11.6 2.5 2 2 2 1000 46. 1440 0.1 1260 6. 28 1.0 110. 1320 10. 1320 10. 1320 10. 10. 10. 10. 10. 1300 11 0.0 1.0 10. 10. 10. 11. 0.0 10. 10. 10. 10. 10. 10. 10. 10. 10. 10. 11.0 10. 11.0 10. 11.0 10. 10. 10. 10. 10. 10. 10. 10. 10. 10. 10. 10. 10. 10. 10. 10. 10. <t< td=""><td></td><td>1420</td><td>10.</td><td>1220</td><td>10.</td><td>95</td><td>1.0</td><td>1260</td><td>7.5</td><td>1220</td><td>10.</td><td>'</td><td>•</td><td></td><td>1</td><td>250</td><td>_=</td><td></td><td>000</td><td>1</td><td>•</td></t<>		1420	10.	1220	10.	95	1.0	1260	7.5	1220	10.	'	•		1	250	_=		000	1	•
1440 0.2 1350 4. 73 1.5 1200 10. 1320 10. 5 0.6 .94 2.6 5 25 1000 667 1470 0.1 1230 10. 18 1.0 1170 10. 1320 10. 5 0.6 .94 2.6 5 25 25 1000 667 1470 0.1 1260 6. 28 1.0 1350 10. 1140 10. 11 0.7 .95 2.3 8 36 36 30 1000 112 1390 5.0 12.0 12.0 11. 36 1.0 600 10. 1230 10. 1230 10. 1230 10. 1230 10. 1350		1470	0.1	1290	<u>ښ</u>	18	0.8	1290	10.	1245	10.	ં			4	22	7		00	46,	1000
14.0 0.1 12.0 12.0 10. 18 1.0 11.0 11.0 11.0 1 11.0		1440	0.2	1350	4,	73	1.5	1200	10.	1320	10.				1	ı	14		000	299	1000
0.1 1260 6. 28 1.0 1140 10. 11 0.7 95 2.3 8 36 30 1000 112 5.0 1270 11. 36 1.0 600 10. 1230 10. - - 2.4 9 >50 B 30 1000 411 0.1 1230 10. 36 1.1 1380 10. 1350 10. 1350 10. 1350 10. 740 15. - - 2.4 9 >50 B 20 8 20 8 30 8 10. 8 30 10. 4 10. 4 0.5 8 30 8 30 10. 30 10. 30 10. 30 10. 4 10. 4 10. 4 10. 4 10. 4 10. 4 10. 30 10. 30 10. 30 10. 30 10.		1440	0.1	1230	10.	18	1.0	1170	10.	1320	10.				2	25	e)		00	8	800
1390 5.0 1270 11. 36 1.0 600 10. 1230 10. - - 2.4 9 500 20 20 1000 411 1440 0.1 1230 10. 36 1.1 1260 10. 1350 10. 13 0.8 1.3 2.8 10 56 20 20 20 20 20 20 1450 0.1 1080 12. 19 .9 1350 10. 740 15. - 0.8 2.8 8 30 64 20 20 1450 0.1 1080 12. 19 .9 1350 10. 740 15. - 0.8 2.8 8 30 64 20 1450 0.1 1270 8.5 13 .8 1290 8. 270 1. - 1.1 2.1 4 - 2 2 2 1450 0.1 1270 8.5 10 .8 1050 10. 960 7.5 - 1.9 4 14 4 3 900 28 1450 0.1 1270 8.5 10 .8 1050 10. 960 7.5 - 1.9 4 14 4 3 900 28 1450 0.1 1270 8.5 10 .8 1050 10. 960 7.5 -		1470	0.1	1260		28	1.0	1350	10.	1140	10.		7		∞	36	(1)		00	112	900
1440 0.1 1230 10. 36 1.1 1380 10. 1350 10. 13 0.8 1.3 2.8 10 5-50 54 16 100 320 1490 0.2 1200 15. 34 1.1 1260 10. 740 15 0.8 2.8 8 30 55 23 700 750 1500 0.1 1080 12. 19 .9 1350 16. 970 23. 4 0.5 0.8 2.0 9 22		1390	5.0	1270	11.	36	1.0	009	10.	1230	10.	-1-	-		6	>50			00	411	740
1490 0.2 1200 15. 34 1.1 1260 10. 740 15. 0.8 2.8 8 30 65 23 700 750 1500 0.1 1080 12. 19 .9 1350 16. 970 23. 4 0.5 0.8 2.0 9 22 21 1440 0.1 360 25. 48 1.2 1200 10. 780 30. 0.9 2.7 22 700 1.1 1450 0.1 1270 8.5 10 .8 1050 10. 960 7.5 - 1.9 4 14 43 900 28 1450 0.1 1270 8.5 10 .8 1050 10. 960 7.5 - 1.9 4 14 43 900 28 1450 0.1 1270 8.5 10 .8 1050 10. 960 7.5 - 1.9 4 14 43 900 28 1450 0.1 1270 8.5 10 .8 1050 10. 960 7.5 - 1.9 4 14 43 900 28 1450 0.1 1270 8.5 10 .8 1050 10. 960 7.5 - 1.9 4 14 4 3 900 28 1450 0.1 1270 8.5 10 .8 1050 10. 960 7.5 - 1.9 4 14 4 3 900 28 1450 0.1 1270 8.5 10 .8 1050 10. 960 7.5 - 1.9 4 14 4 3 900 28 1450 0.1 1270 8.5 10 .8 1050 10. 960 7.5 - 1.9 4 14 4 4 3 900 28 1450 1.1 1270 1.1 1.1 1.1 1.1 1.1 1.1 1.1 1.1 1.1 1.1 1.1 1.1 1.1 1.1 1.1	_	1440	0.1	1230	10.	36	1.1	1380	10.	1350	10,	ف	œ		10	>50			00	320	800
1500 0.1 1080 12. 19 .9 1350 16. 970 23. 4 0.5 0.8 2.0 9 22 \frac{2}{3} \frac{2}{3} \frac{11450}{3} \frac{1}{3} \f		1490	0.2	1200	.51	34	1.1	1260	10.	740	15.	<u></u>	ं		•	30		23	700	750	009
1490 0.1 780 5.5 13 .8 1290 8. 270 1 1.1 2.1 4 - 5 - 33 1440 0.1 960 25. 48 1.2 1200 10. 780 30 9 2.7 - 3 - 3 - 3 - 3 - 3 - 3 - 3 - 3 - 3 -	2	1500	0.1	1080	12.	19	6.	1350	16.	970	23.		Ś		0	22	W	,		21	979
1440 0.1 960 25. 48 1.2 1200 10. 780 309 2.7 2 22 700 1.7 1450 0.1 1270 8.5 10 .8 1050 10. 960 7.5 1.9 4 14 43 900 28 (a) 1.9 4 14 43 900 28 (b) 1.9 4 14 43 900 28 100 1.9 4 14 43 900 28 100 1.9 100 100 100 100 100 100 100 100 100 10	~	1490	0.1	780	5.5	13	∞.	1290	80	270	, ni		<u> </u>		4	ı	TO	•		33	100
1450 0.1 1270 8.5 10 .8 1050 10. 960 7.5 1.9 4 14 43 900 28 (a) - 1, -1 error (b) - 1, -300 error (c) - 1, -300 error (c) - 1, -300 error (d) - 1, -300 error (e) - 1, -300 error (f) - 1, -300 error (g) - 1,	. 3	1440	0.1	096	25.	48	1.2	1200	10.	780	30.		•		ı	1		22	00/	1.7	400
(a) - 1 - 1 agent (b) - 1 - 200 agents		1450	0.1	1270	8.5	22	∞.	1050	10.	096	7.5				4	14		£	90	28	909
(a) - 1 _p - 1 aspere (b) - 1 _p - 900 asperes																		<u> </u>			
(a) - 1 _y - 1 aspere (b) - 1 _y - 900 asperes													****								
(a) - 1 _p - 1 ampere (b) - 4 _p - 900 amperes																					
TARTE	IR			┤.								1	-	-				1	-		
		3	- 80 · 1						r												

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DEVICED'B" DATA SHEET

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DEVICE "B" DATA SHEET	Ty = 125°C ± 3° Ty = 25°C ± 3° Ty = 125°C ± 3°	BR)RC $V(BR)$ PO $V(BR)$ PO V_{GI} $V_$	1350 10. 39 1.2 1.6 3.2 16 1000 5000	1290 10. 21 1.0 1.6 3.0 10.2 550 17 1000 250	1350 10. 14 .8 1.0 2.4 17.0 >50 25 1000 625	1320 10. 26 1.1 1.2 2.2 22 900 45	920 10. 18 0.8 1.4 2.8 12.0 >50 20 800 320	330 2.5 1.5 3.0 22	450 20. 25 1.0 1.8 2.2 24.0 12	1410 10. 33 1.0 1.0 2.6	640 15. - - 1.0 2.9 - <	11110 35.	1380 20 2.2 16 1000 166	390 10 1.0 3.0 13.0 40 30 150 66	1260 7. 10 0.7 .9 2.2 10.8 >50 48 1000 31	810 15	1360 25 333	1365 10.	1350 9. 12 0.8 1.2 2.5 11.2 43 5 18 1000 333	1120 10. 19 1.0 1.3 2.4 17.0 50 50 1000 1667	660 50. 17 1.0 1.6 3.0 25.0 28 \frac{12}{24} 12 500 115	270 50 1.6 3.8 -	460 25 1.1 2.9 9.0 - E 13 400 50	885 12. 7 0.6 1.2 2.2 22.0 20 2 - - 140	600 10 1.0 2.6 5.6 - 22 400 50				
DEVIC		VGT OT TO	1.6 1260 1	1.2 1350	1.2 1200	1.6 1320	1.1 1240	1.3 1350 10	1.4 1290	1.4 1380	1.2 1350	1.4 1230	1.5 1390	1.0 1350	1.1 1320	1.3 1360	1380	1.5 1290	1.2 1290	1.2 1380	1.7 1200	1.2 1110	1.0 1170	1.1 1200	p. 9 1230			_	
1	- 25°C ± 3°	V(BR)FO 1(BR)FO LGT	10.	2.		ri.	.5.	330 0.2 58	10.	25.	25.	25.	20.	0.1		10.	25.	10.	10.	ж о	٠,		25.	12.5	10.		 _	_	
E-79	H.	(BR)RO (BR)RO or or or or						1490 0.1														1060 10.					 -	,	· · · · · · · · · · · · · · · · · · ·
iot 180.		H 3740	-					9	_	∞												50				 		_	

	P.	18	- 8	-8		- 0		Ď	-							·					
	1	-						25	74		·		·	 -			٠				
, * 3°	d(vp)	3333	233	333	•	50	•	192	300											 	
125	8	1000	700	1000	300	300	906	250	400								·····				
•	t off	28	43		25	18	39	22	15				*******				·				
	T _B D								EASURED	W.	LON										
	rg B	8	09	100	30	15	7	19	13							·					
- 44	o o								EASURED	W i	LON										
2.5	₽ 9	•	2.2	2.4	2.5	2.8	3.0	2.6	2.8									······································			
	⊳ r	1		_																	
	A _{GT}		· ·	1.2	1.5	1.0	٠.	·-													
	, to	20	10	29	20	∞	14	9	7												
	(BR)FO or fro	8.0	10.	10.	10.	10.	10.	10.	10.												
25°C ± 3°	BR)FO	1395	840		510	495	1140	330	510			·		····							
1.7	ļ			· · · ·										·-·							TABLE 7
	1 (BR)RC or 1 RO	10	10	10	10	10	10	10	10												IAI
	(BR)RO or RO	1380	1200	1320	450	450	1185	1200	1200					**************************************				· · · · · · · · · · · · · · · · · · ·			
	4 GT	1.3	1.2	1.4	1.8	∞.	0.1	1.1	0.0										\dashv		
	i.	58				18		9								·····			1		
	1(BR)FO or 1 ₇₀	10	10	10	10	10	10	10	10												
• 25°C ± 3°	*(BR)FO or *FO	1260	885	1260	1140	1020	1260	450	099												
1,	(BR)RO or ¹ RO	.1	۲.	۲.	10.	10.	5.	.2	7.											• 1 espera • 90 espera	
	(BR)RO or RO	1500	1380	1440	1500	1140	1500	1110	1100									<u>,</u>	7	1 1	•
21,	१ ३१५०	-	7	7	2	9	12	14	16												
	t ₃ = 25°C ± 3°	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$			Tennen Total series Total series	TJ = 25°C ± 1° VBR)RO 4 (BR)RO <td>Versible Image: Legic state sta</td> <td>Very Inc. I_{CR} In</td> <td>Very No. Long N</td> <td>Very libral Light Indicated and in</td> <td>Verify to 1500 1.0 (a) (a) (a) (a) (b) (b) (b) (b) (b) (b) (b) (c) (a) (b) (c) (b) (c) (c) (c) (c) (c) (c) (c) (c) (c) (c</td> <td>$\begin{array}{c c c c c c c c c c c c c c c c c c c$</td> <td>$\begin{array}{c c c c c c c c c c c c c c c c c c c$</td> <td>$\begin{array}{c ccccccccccccccccccccccccccccccccccc$</td> <td>$\begin{array}{c c c c c c c c c c c c c c c c c c c$</td> <td> The color The</td> <td>Vanish Lange of the control of the contr</td> <td>$\begin{array}{c c c c c c c c c c c c c c c c c c c$</td> <td>$\begin{array}{c ccccccccccccccccccccccccccccccccccc$</td> <td>$\begin{array}{c ccccccccccccccccccccccccccccccccccc$</td> <td>$\begin{array}{c ccccccccccccccccccccccccccccccccccc$</td>	Versible Image: Legic state sta	Very Inc. I_{CR} In	Very No. Long N	Very libral Light Indicated and in	Verify to 1500 1.0 (a) (a) (a) (a) (b) (b) (b) (b) (b) (b) (b) (c) (a) (b) (c) (b) (c) (c) (c) (c) (c) (c) (c) (c) (c) (c	$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	The color The	Vanish Lange of the control of the contr	$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$

4	. B1							DEVICE	B DATA	DATA SHEET					1-4	\$ \$	30	30 April	1963	
4			T, - 25°C ± 3°					T	T, = 125°c ± 3	30			L.	Ty = 25°C ± 3°			T,	, = 125°C ±	: # 30	
H STUD	*(BR)RO or *RO	1(BR)RO or 1RO	(BB)FO or FO	1(BR)F0 or 1 _{F0}	1 _G T	T _O	V(BR)RO or VRO	1(BR)RC or ¹ RO	V(BR)FO or VFO	(BR)FO or f _{FU}	LGT	V _{GT}	γ _F γ _F (a)	G on	L BO	I B	toff Tapp	dd*	q(xb0)	dd∎
1	1395	10	1170	10	10	ω.	1080	15	066	20	4	٠٠.	1.1 2.4		17		22	800	129	800
9	1290	10	720	24	14	٥	066	25	410	14	m	9.	1.0 2.8	~	25		25	300	58	300
7	1260	10	1170	10	55	1.2	1110	15	1110	15	26	1.0	2.5 -		80		12	005	180	900
)6	() 1140	10	1020	80	17	10	840	25	720	22	9	9.	2.0 -		12		10	009	150	009
10	6) 870	25	1110	7	10	∞.	840	25	750	25	9	9.	1.2 3.4		7		19	009	10	009
11 (6)	c) 1260	10	1110	7	80	۲.	1170	1.5	009	∞	2	٠,	1.2 3.0		7.9	*********	13	200	6	500
12	1080	10	096	9	94	1.3	1170	10	1050	7	20	∞.	1.1 2.6	וצבו	35	иер	15	800	138	800
13	1065	۲.	1050	16	42	1.2	1170	10	1110	10	20	1.0	1.2 2.8		09		16	006	161	006
14	1120	10	1020	12	51	1.2	1215	10	840	00	21	∞.	1.1 2.7		80		15	200	121	700
115	1500	7.0	1320	7	38	1.1	1110	10	1140	10	14	.7	1.1 2.4		100		35	900	180	006
16	1455	۲.	1260	10	29	1.4	1080	10	1140	10	26	6.	1.2 2.8	~	09		28	006	1800	006
17	1410	۲.	1230	10	9/	1.6	1365	10	1350	10	37	1.2	2.0 -		140		15 ‡(000	2500	000
18	1470	7.	1275	e	14	∞.	1335	10	1170	∞	7	٠.	.8 1.7		17		1	400	17	400
19	1440	.2	780	6	9		1350	10	510	6	7	7.	.8 1.8	•	7		,	<u> </u>	,	,
70	1320	10	1200	10	21	٥.	1245	10	1020	∞	6	9.	1.0 2.0		21		<u> </u>	800	107	800
21	1470	e.	1140	10	10	.7	1260	10	780	6	m	∞.	.8 1.9		4		t	1	4	009

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							v										· · · · · · · · · · · · · · · · · · ·			
	1 (0) -1	. 1																		

FORM: (a) -1_p = 1 ampers (b) -1_p = 500 ampers (c) -- Gold Diffused

$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		dde /	700	009	000	000	009	200	200	200	006	700		
Transmo '(max) (max) (ma	°C * 3°		23	15	312	200	40	83	01	16	7.5	87		
Transcript (1837) Transcript (1	Ty = 125	ddw _ /JJ												
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$						_,								
Very the property of t			12	2	08	17	9	<u>۾</u>	15					
Vanish T_{exp} = $2x^{5}$ C s x^{5} T_{exp} = $3x^{5}$ C s x^{5} T_{exp} = $3x^{5}$ C s x^{5}	++	8	2				4.5			4.0				
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		h 3	6:	· ·	.3	5.5	0.2	2.4	2.3	2.5	3.4	3.6		
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		Þ 4 €								.94				
The property of the propert		72	5.		0.1	٥.	٠.	0.1			9			
T ₁ = 25°C ± 3° Year)ind Again and A		ţ,	4				n		9	4	7	9		
Version of term in the control of term in th		1(BR)FO or 1FO	5.0				6.0		4.0	4.0	6.0	8.0		
T _J = 25°C z ± 3° V(RR)NO * (RR)NO * (RR)	+1	(BR) PO or	098	740	1340	1200	760	079	620	979	1100	840		į.
T _J = 25 ^o C ± 3 ^c T _D (RR)NO (RR)NO (TER)NO (TER)			10	10	10	10	10	10	10	10	10	10		į
T _J = 25 ^o C ± 3 ^c T _D (RR)NO (RR)NO (TER)NO (TER)		(BR) NO	1260	1540	1320	1400	1400	1420	1280	1320	1360	1260		
T3-25°C # 3	-	ļ	 ∞	٦.	7.	1.1	۲.		σ.	∞.	.95	1.1	· · · · · · · · · · · · · · · · · · ·	
The state of the s			12	25	73	76	9		14	6				
(88) NO (88) N		 	10.0	3.0	٠.	7.0	10.0	10.0	5.0	9.0	'n	10.0		
(88) NO (88) N	- 25°C ± 3°	(BR) FO	1280	1180	1280	1260	1120	800	1100	1060	1160	1040		
	4		0,	.02	.2	.03	.05	.05	3.0			.2		- 1 ampare
10 9 8 7 6 5 4 3 5 1 mit ht		(BR)RO or	380	1420	1320	1300	1400	1340	1280	1240	1320	1200		(a) - I, - 1 ampare
		4H 174N	+-	- 7	. m	4	٦	9		. 00	, 6	10		50

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30 April 1963

	dd.	700	300	700	1
T, = 125°C ± 3°	d(vpo)	116	23	116	
ă - '.	toff / *pp	700	1	700	
	of t	129	1	15	
_	I BD	24	9	50	1
	L S	13	4	11	
. 25°C ± 3°	G OH	5.5	4.3	7.	
T. 2	№ 9	1.2 2.9 5.5	. 771.6 4.3	2.7	
	₽ (e)	1.2	. 77	1.2 2.7	
	V _{GT}		ı	1	
	15		,	•	
	1(BR)FO or 1FO	10	9	10	
Ty = 125°C ± 3°	V(BR)FO or vF	780	740	089	TABLE 10
T,	L(BR)RC or LRO	10	10	10	TAT
	(BR)RO or 'RO	.9 1200	.8 1360	1.1 1200	
	TO GT	9.	ω.	1.1	
	į.	24	14	38	
	¹ (BR)PO or ¹ PO	10	10	10	
T, - 25°C + 3°	(BR)FO or	006	1000	800	
1.	1(BR)RO or 1RO	0.1	0.08	8.0	1, = 1 aspere 1, = 500 asperes
	*(BR)RO or *RO	1100	1280	1120	11
1	H STWA	25	95	65	
		٠			,

Date 30 April 1963

DEVICE "B" DATA SHEET

Lot No.

MORES: (a) - I_p - 1 apers (b) - 1_p - 500 apers (c) -- 601d Diffused

T _J - 25 ^o c + 3 ^c Table Table <t< th=""><th>TOT ATT</th><th>DAIR SIEEL</th><th></th><th>Date 30 April</th><th>1963</th></t<>	TOT ATT	DAIR SIEEL		Date 30 April	1963
*(PRN)*TO *(PRN)*TO <t< th=""><th>Ty = 125°C ±</th><th>± 3º</th><th>T, = 25°C ± 3°</th><th>t₁ = 125°C ±</th><th>و ۽ ع</th></t<>	Ty = 125°C ±	± 3º	T, = 25°C ± 3°	t₁ = 125°C ±	و ۽ ع
120 .6 19 1.1 600 10 1340 1.0 10 .75 1300 10 1300 .1 23 1.1 1200 10 1300 .1 23 1.1 1200 10 1300 .02 13 .8 1540 10 1300 .02 13 .8 1540 10 1300 3.0 14 .7 1480 10 1160 .1 5 .65 1360 10 1160 .5 5 .7 1480 10 1160 .5 5 .7 1480 10 1160 .7 48 1.1 840 10 1160 .1 34 1.1 840 10 1160 .1 34 1.1 840 10 1160 .2 44 1.1 6 640 10 <t< th=""><th>A(BR)RC or</th><th>t (BR)FO LGT FGT</th><th>T (z) (b) to D T T T T T T T T T T T T T T T T T T</th><th>In tore Tape</th><th>dow / oda</th></t<>	A(BR)RC or	t (BR)FO LGT FGT	T (z) (b) to D T T T T T T T T T T T T T T T T T T	In tore Tape	dow / oda
1340 1.0 10 .75 1300 10 1300 .1 23 1.1 1200 10 1200 .02 13 .8 1540 10 1200 .02 13 .8 1540 10 1200 3.0 14 .7 1480 10 1200 3.0 9 .7 1460 10 1160 .1 5 .65 1360 10 1160 .5 5 .7 1380 10 1160 .1 5 .7 1380 10 1160 1.3 60 1.5 1360 10 1160 1.3 48 1.1 840 10 1060 1.3 34 1.1 840 10 1160 2.0 38 1.0 440 10 1140 1.0 31 1.0 10 1160 1.0	00 10	3.0	.96 2.0 5.8 5	. 8	•
4 1300 .1 23 1.1 1200 10 5 1200 .02 13 .8 1540 10 5 1200 3.0 14 .7 1480 10 5 1200 3.0 .7 1480 10 3 1160 .1 5 .65 1360 10 3 1160 .5 .7 1380 10 10 1160 .5 .7 1380 10 10 10 1160 1.3 60 1.5 1360 10 10 10 1060 .1 34 1.1 840 10		3.0 -	.82 1.8 4. 2	- 001₹ 7	14 700
1200 .02 13 .8 1540 10 1300 3.0 14 .7 1480 10 1200 3.0 9 .7 1460 10 1140 .1 5 .65 1360 10 1160 .5 5 .7 1380 10 1160 .5 6 1.5 1360 10 1160 1.3 60 1.5 1400 10 1160 1.3 48 1.1 840 10 1000 .1 34 1.1 840 10 1000 .1 34 1.1 840 10 1160 2.0 38 1.0 640 10 1140 1.0 31 1.0 640 10 1140 1.0 31 1.0 640 10 1160 .3 1.0 560 10 1160 .3		6.0	.99 2.0 4.5 4	11 26 800	43 950
1300 3.0 14 .7 1480 10 1200 3.0 9 .7 1460 10 1140 .1 5 .65 1360 10 1160 .5 5 .7 1380 10 1160 3.0 - - 1400 10 1140 1.3 60 1.5 1360 10 120 1.3 48 1.1 840 10 1060 .1 34 1.1 840 10 1060 .1 34 1.1 840 10 1060 .1 34 1.1 840 10 1060 .1 34 1.1 840 10 1160 2.0 38 1.0 640 10 1140 1.0 31 1.0 10 1140 1.0 31 1.0 10 1160 .3 1. <			- 70 1.6 4.8 -	1	
.05 1200 3.0 9 .7 1460 10 .03 1140 .1 5 .65 1360 10 .03 1160 .5 5 .7 1380 10 .4 1160 3.0 - - 1400 10 .3 1140 1.3 60 1.5 1360 10 .9 120 1.3 48 1.1 840 10 .9 1000 .1 34 1.1 840 10 .7 1060 3.0 53 1.2 960 10 .7 1060 3.0 53 1.0 640 10 .6 1160 2.0 44 1.1 620 10 .6 1160 3.1 1.0 560 10 .7 1160 .3 1.0 34 10 .7 1160 .7 940 10		1.5	.72 1.5 4. 2	3	2.5 200
.03 1140 .1 5 .65 1360 10 .03 1160 .5 5 .7 1380 10 .4 1160 3.0 - - 1400 10 .3 1140 1.3 60 1.5 1360 10 .9 120 1.3 48 1.1 840 10 .0 1000 .1 34 1.1 840 10 .7 1060 3.0 53 1.2 960 10 1.0 720 5.0 38 1.0 640 10 1.0 1160 2.0 44 1.1 620 10 1.0 1140 1.0 31 1.0 560 10 4 1260 .3 6 .7 940 10 .2 1160 1.0 2 10 10 10 .3 10 8 .7 <td></td> <td>1.4</td> <td>.73 1.9 4. 2</td> <td>3 -</td> <td>•</td>		1.4	.73 1.9 4. 2	3 -	•
.03 1160 .5 5 .7 1380 10 .4 1160 3.0 - - 1400 10 .3 1140 1.3 60 1.5 1360 10 .9 120 1.3 48 1.1 840 10 .06 1000 .1 34 1.1 840 10 .7 1060 3.0 53 1.2 960 10 .6 1160 2.0 44 1.1 620 10 .6 1160 2.0 38 1.0 640 10 .6 1160 2.0 44 1.1 620 10 .7 1160 1.0 31 1.0 560 10 .7 1160 1.0 2 1.0 10 10 .7 1000 1.0 8 .7 860 10 .7 1000 1.0 <td< td=""><td></td><td></td><td>.83 2.4 4. 2</td><td>2</td><td>1</td></td<>			.83 2.4 4. 2	2	1
.4 1160 3.0 - - 1400 10 .3 1140 1.3 60 1.5 1360 10 .9 120 1.3 48 1.1 840 10 .06 1000 .1 34 1.1 840 10 .7 1060 3.0 53 1.2 960 10 1.0 720 5.0 38 1.0 640 10 1.0 1160 2.0 44 1.1 620 10 1.0 1140 1.0 31 1.0 560 10 .4 1260 .3 6 .7 940 10 .5 1160 1.0 21 1.0 10 10 .5 1000 7.0 8 .7 860 10		1.3	.85 2.5 4. 2	٦ ١	7.5 600
.3 1140 1.3 60 1.5 1360 .9 120 1.3 48 1.1 840 .06 1000 .1 34 1.1 840 .7 1060 3.0 53 1.2 960 1.0 720 5.0 38 1.0 640 .6 1160 2.0 44 1.1 620 1.0 1140 1.0 31 1.0 560 .4 1260 .3 6 .7 940 .2 1160 1.0 21 1.0 1080 .5 1000 7.0 8 .7 860		4.0	4.8	7	16 900
.9 120 1,3 48 1.1 840 .06 1000 .1 34 1.1 840 .7 1060 3.0 53 1.2 960 1.0 720 5.0 38 1.0 640 .6 1160 2.0 44 1.1 620 1.0 1140 1.0 31 1.0 560 .4 1260 .3 6 .7 940 .2 1160 1.0 21 1.0 1080 .5 1000 7.0 8 .7 860		3.0	.93 2.4 8. 2	6 35 600	4 600
6 1000 .1 34 1.1 840 1060 3.0 53 1.2 960 720 5.0 38 1.0 640 1160 2.0 44 1.1 620 1140 1.0 31 1.0 560 1260 .3 6 .7 940 1160 1.0 21 1.0 1080 1000 7.0 8 .7 860		2.0 -	2.0 4.2 7.5 18	35	•
1060 3.0 53 1.2 960 720 5.0 38 1.0 640 1160 2.0 44 1.1 620 1140 1.0 31 1.0 560 1260 .3 6 .7 940 1160 1.0 21 1.0 1080 1000 7.0 8 .7 860		10.0	1.0 2.4 4.8 9	21	
720 5.0 38 1.0 640 1160 2.0 44 1.1 620 1140 1.0 31 1.0 560 1260 .3 6 .7 940 1160 1.0 21 1.0 1080 1000 7.0 8 .7 860		10.0	1.5 3.8 6.2 12	24 5 900	006 006
1160 2.0 44 1.1 620 1140 1.0 31 1.0 560 1260 .3 6 .7 940 1160 1.0 21 1.0 1080 1000 7.0 8 .7 860		10.0	2.2 5.8 7.0 5	12 7 400	200 400
1140 1.0 31 1.0 560 1260 .3 6 .7 940 1160 1.0 21 1.0 1080 1000 7.0 8 .7 860		10.0	2.3 5.0 8.5 7	13 20 400	200 400
1260 .3 6 .7 940 1160 1.0 21 1.0 1080 1000 7.0 8 .7 860		10.0	1.9 4.2 7. 6	17 11 400	333 400
1160 1.0 21 1.0 1080 1000 7.0 8 .7 860		2.0	83 2.0 4.8 3	E	
1000 7.0 8 .7 860		10.0	1.1 2.8 6. 3	12 25 400	22 400
		5.0	.85 2.0 3.8 2	7	1
		1		1	

1																			
		/***	•	8	8	3	8	8	3	•	8	•	8	8	8				
36 April 1963	1, - 125c - 1°	(4)	•	1800	3	240	1000	3	20	•	430	•	346	5 0	180	•			
124	3		•	8	•	000	8	•	•	•	8	•	8	•	3	,			
2	•	والأريف	•	ជ	•	28	21	1	•	•	22	•	17	•	27	,			
å		T.	٠	17	•	=======================================	2	2	60	•	0	•	2	1	7	1			······
		g,	1	7	•	m	4	11	~	٠	9	•	9	7	~	1			
	ب، عرده ه	*o ••	•	7.0	10.0	6.3	6.5	7.0	6.0	5.8	6.0	•	8.0	5.0	5.0	•			
	3	* 3	6.6	3.7	3.2	3.5	3.7	2.9	3.6	3.8	0.	5.4	6.0	2.6	3.7	5.6			
į		7	1.7	1.5	1.2	1.2	1.2	1.1	1.1	1.2	1.1	* :	1.3	.9	H. 0	1.4			
		4	•	•	•	•	•	•	•	•	•	•	•	•	•	•			
		ď,	•	•	•	•	•	•	•	•	,	•	•	•	•	•			
DATA SREET		os(m),	10.0	10.0	9.0	8.0	4.0	8.0	4.0	5.0	6.0	6.0	10.0	2.5	1.8	9.0			
	2, - 325c = 5	or(m)	1240	1120	1220	1200	99	120	9%	8	1380	820	3	240	3	627	- Animali I	<u>-</u> -	18-2-4
DEVICE	3	Castas).	10.01	10.0	2.0	10.0	5.0	10.0	10.0	10.0	10.0	0.01	10.0	10.0	10.0	15.0			
		OI (16)	1320	1300	320	1380	36	1360	1320	1240	1480	1360	1320	1500	1400	1260		,	
		, ii	1.2	1.1	2.4	1.5	1.3	1.2	1.4	6.0	1.2	2.6	2.6	6.0	B.				
		Į.	35	ม	2	8	2	33	33	92	33	2	2	2	==	*			
		2 · F	0.2	2.0	4.0	0.7	2.0	5.0	\$	9.6	0.03	3.0	10.0	4.0	0.1	1.0			
1	2, - 18 e 5	ega, e	1160	1160	1120	1200	1160	180	1080	8	1240	3	1180	992	36	3			
	3	e i	0.2	0.07	0.3	0.05	0.02	0.03	6.1	9.13	e. 8	9.06	0.3	\$	9.93	0.2			
2		9 . a	1320	1300	8	1300	220	1420	1360	1320	1420	385	1400	1380	1400	1300			
á	T	1 1141	-	~	•	4	n	•	^		•	2	#	77	מ	7.			

P. Santana . Pr. Called .

Then, py the py	1		7 6	, -							
The color of the			•	·		200	200		950	950	1
The property of the property	1963	0.	(Pa)	#	•	25	22	220	118	126	
The property of the property	pril		9	:	1	•	200				-
The property of the property	30 A	•	t of i			∞					
The state of the s	Date S		I B		9	<u>۰</u>	4 0	14	11	11	
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$					7 (2 0	v ~	n •	9	2	
The state of the		- ++	0				4 .r.	5.5	4.5	6.0	
T ₁ = 25°C ± 3°C = 1°C			, , ,	9 9	2.0	2.0	2 . 3	2.3	2.5	2.5	
Carlo Carl		_	Þ. (3	9 9	o 0	<u>,</u> 0	· -	1.0	1.0	<u>.</u>	
T, -25°c s f					:		,	1	ı	1	
The state of the			r ₂		·		,		,		
The state of the		0_	1(BR)FO or	2 2	· ·	j r	4.0	7.0	8.0	9.0	
The state of the		125°C ±		2,	2,0	1040	1000	1300	1320	1280	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		£.	1(BR)RC or	02 C	2 5	2 0	10	10	10	01	
T _J = 25°C a 3° V(BR)RO V(BR)PO $^{1}(BR)PO$ $^{1}(BR)PO$ $^{1}(BR)PO$ or ^{1}EO ^{1}EO ^{1}EO ^{1}CO 1380 0.5 100 0.3 12 1280 0.01 1140 0.01 12 1360 0.05 1200 0.6 26 1360 0.03 1200 0.08 27 1440 0.05 1200 0.06 30 1440 0.04 1200 0.6 30 1400 0.04 1200 0.6 30 (*) - 7-1 aupore			(BR) RO	1,000 1,000	1360	1440	1280	1420	1440	1400	
T _J = 25°C a 3° V(BR)RO V(BR)PO $^{1}(BR)PO$ $^{1}(BR)PO$ $^{1}(BR)PO$ or ^{1}EO ^{1}EO ^{1}EO ^{1}CO 1380 0.5 100 0.3 12 1280 0.01 1140 0.01 12 1360 0.05 1200 0.6 26 1360 0.03 1200 0.08 27 1440 0.05 1200 0.06 30 1440 0.04 1200 0.6 30 1400 0.04 1200 0.6 30 (*) - 7-1 aupore			T GT	\alpha	7		6.	0.	0.	٦.	
The state of the			L.							о Д	
T _j = 25°C ₂ T _j = 25°C ₂ T ₀			¹ (BR)FO or								
(a) - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 -	1	- 25°c ± 3°	(BR)FO	100	1140	1200	1100	1200	1200	1200	
(a) - (b) - (c) -		T,		\dagger	0.01	0.05	0.02	0.03	0.02	0.04	- 1 aspere - 500 asperes
5 TH 21MU 1 4 4 70 7 7 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1		(BR)RO or	1380	1280	1360	1160	1360	1440	1400	
	lot Bo.	J.	र अग्यत	-	2	٣	7	2	9	_	ë

DEVICE "B" DATA SHEET

Lot No. P7

	1	dá	900		<u></u> .			
2		1	18					
30 April 1963	Ty = 125°C ± 3°	d(vin)	180	1	,	•	e.	
Apr	2	torr / app	900		,	•		
8	-	, s	12	ı	•	ı		
3 2		ř. Ed	ı	15	ı	4		
		L CE	22	9	•	2		
	Ty - 25°C ± 3°	G OB	12	4.5	4.2	3.5		
	1, 2	₽ ⊕	6.4	3.2	2.5	2.4		
) 	γ (<u>a</u>)	2.0 6.4	1.1 3.2	.92 2.5	.87 2.4		
		V _{GT}	,	1	,	,		
		Į.		,	,	,		
DATA SHEET		1(BR)FO or 1 _{FO}	10	1.3	ı	3.0		
	T, = 125°C ± 3°	*(BB)FO or *FO	500	70	ı	720		TABLE 14
DEVICE B	et 19	1(BR)RC or 1RO	10	10	5.0	10.0		TABL
		*(BR)RO or *RO	1280	1300	320	1320		
		V GT	1.9	٥.	۰.	9.		
		Let	19	14	9	2		
		¹ (BR)FO or ¹ FO	10	2.0	,	4.0		
1	T, - 25°C ± 3°	*(BR)FO or *PO	009	09	10	1040		
	T,	(BE)EO or 1EO	.3	.08	6.0	.05		1, - 1 aspere 1, - 500 asperes
P8		*(BR)RO or *RO	1200	1240	200	1220		(E) (C) (C) (C) (C) (C) (C) (C) (C) (C) (C
lot 16.	4	१ ३३५०	1	7	e	4		
-								

Ict 16. P10

Date 30 April 1963

T	dd* /	700	900	000	3 8	5 6	000	000	800	800	006	006	1	800		
T, - 125°C ± 3°	d(vro)	700	900	750		250	800	40	133	133	450	90	•	22		
1.25	od.					*******			KED	USA	WE	TON				
	toff / Tapp								KED	USA	WE	TON				ı
	1 ED								KED	USA	ME	TON				
	<u>1</u>	25	\$	2	0 ;	14	28	14	11	15	35	11	∞	9		
0 ± 3	a S	20	15	9	01	σ	14	17	9	9	8.5	9	5.5	Ŋ		
Ty - 25°C	₹	2.2	5.8	,	7.+	7.7	4.7	4.0	4.2	2.4	4.2	2.3	2.2	2.5		
•	⁴ €	,	<u>۔۔۔</u> لخ		γ γ	1.8	2.2	1.5	1.8	1.2	.4 1.9	1.1	.97	.97		
	4 2	1.8	1.8				1.5	1.5	,	9.	1.4	.7	.5	ئ.		
	ţ,	47	42			14	33	20	,	10	26	10	7	ω		
	1(BR)FO or 1 _{FO}	10	2,5		0.0	10	10	8.0	10	2.0	10	5.0	4.0	4.0		
• 125°c ± 3°	(BR)FO or PFO	880	1180	20 0	1260	840	1100	086	1100	920	1220	1120	1020	1020	<u>and an entire property of the second of the</u>	
T _J	1 (BR)RC or 1-RO	10		2 ;	01	10	10	10	10	10	10	10	10	10		
	(BR) RO	1380	1320	1360	1340	1020	1050	1080	1060	1200	1240	1300	1280	1320		
	, to	3 2		?	2.8	1:1	3.0	3.7	1.0	6.	2.1	1.1	6.	.85		
	, E	250			93	746	250	150	22	27			22	23		
	L(BR)PO		ç	50.	.02	.2	80.	۲.	٦.	2.0	80.	.05	۳ <u>.</u>	40.	·	
T3 - 25°C + 3°	(BE)FO	1060	20 0	1000	1140	1120	1120	1180	1160	1120	1120	1200	1100	1160		
T.	1(BR)HO	2 5	<u> </u>	.03	.05	.5	m.	۳.	۳.	2.0		.05	80	90.		I 1 aspera
	(BR)RO or	2 3	0007	1240	1280	1240	1220	1300	1280	1240	1200	1260	1240	1260		3
<u> </u>	ch stau	+	_	7	<u>س</u>	4	~	•	7	α	, 5	12	71	15		Ë

NOTES: (a) - $\frac{1}{7}$ - 1 aspers (b) - $\frac{1}{7}$ = 500 asperse

		ddr.	1	'	
30 April 1963	T _J = 125°C ± 3°	d(v ₇₀)	1	1	·
Apr1	521 -	gd.	1000	1000	
	F.	toff ' app	100 1000	≻ 100 1000	
Date		Œ _I	,	ı	
		T _{EO}	,	1	
	t, - 25°C ± 3°	a g	ı 	•	
	2.	٠ <u>.</u> ع	1.9	.75 2.0	
		γ (e)	.75	.75	
		Tt P	1	1	
		į	1	1	
DATA SHEET	0	1 (BR) FO or 1 FO	20	15	
	Ty = 125°C ± 3°	(BB)PO or PO	1020	1400	
DEVICE B	r,	1(BR)RC or 1-RO	70	10	
		(BR)30 or BD	1120	1600	
		• GT	ω.	1	
		Į.	10	,	
		1(BR)FO er 1 _{FO}	10	۲.	
1	1 - 25c + 3c	V(BR)PO or VPO	1180	1360	
CONTROL		(88) Car (88)	2	۲.	
BT-30		(BR)RO or	1180	1600	
ž Š		H 3740	-	7	

1963	t 3°	d(vpg) / app	,	1	1	,	1		· ·	1	2500 1000	2250 900	2250 900	2500 1000	330 300	2500 100d	1500 600		
30 April 1963	Ty - 125°C + 3°	toff Tapp di	47 100d	1000	1000	1000	1000	1000	1000	1000	006	- 22	906	900	1	- 25	009		
	-		47	29	29	30	31	26	25	29	25	1	32	35	1		25		
Date		Teo Teo	·					_	······	15	30		32	34	TOF	····	31		$\frac{1}{2}$
	ص	on I	. 1			<u> </u>	•		-		<u>~</u>			<u>~</u>		•			1
	• 25°C ±	* _G		1	1	1	1	1	<u> </u>	3.5	<u>61</u> ∞	1	5.5	٦.		ره .	7.5		
	,	(d)	3.2	1.453.3	1.323.4	1,413.5	1.453.4	1.3 2.9	1.552.9	1.353.1	2 2.7	1.122.4	252.7	192.7	1	1.092.45	71.252.5		-
		T (a)	1.2								1.31.2 2.75		0.81.252.7	0. 71. 152. 7	1	<u>;</u>	71.		$\frac{1}{2}$
		fer ver	1	1	-	1	<u>'</u>	ı	-	<u> </u>							<u>.</u>	· · · · · · · · · · · · · · · · · · ·	$\left\{ \right.$
F(. !	1	. 1	!	1	1	_!	_!_	9	!_	16	119			14		$\frac{1}{1}$
DATA SHEET	30	(BR)FO or fro	12	20	20	20	20	20	70	20	20	25	25	25	20	25	21		
	Ty = 125°c ± 3°	*(BB)FO or *FO	1280	1280	1200	1280	1350	1360	1400	1240	1100	1040	1040	1120	360	1080	720		
DEVICO'B"	1	1(BR)RC or ¹ RO	20	20	20	20	20	20	20	20	25	25	25	25	25	25	25		
		*(BR) RO or PHO	360	1260	360	1100	1350	1320	1400	1240	1140	1080	1040	1120	260	1120	1180		
		VGT	1.1	1.0	1.0	ਜ:	1.4	1.5	1.2	1.4	2.0	١	1.2	1.0	i	1	1:1		
		LoI	20	70	20	30	45	0	4	30	91		36	9	1	1	30		
		1 (BR) PO or 1 Pro	10	10	10	7	10	10	10	10	10	10	10	10	10	10	٧		
sed	1 = 25°C * 3°	(BR)FO or PO	1500	1390	1340	1260	1400	1500	1420	1260	1320	1200	1220	1300	8	1260	1000	·	
BT-30 AuDiffused	I.	(BR)RO or 1RO	10	10	10	10	01	10	10	10	10	10	10	10	10	10	10		
ł		(BR)RO or RO	120	1400	240	1200	1400	1520	1420	1240	1320	1200	1160	1260	130	1240	1120		
lot lo.		4 37 4 0	г	2	4	2	9	7	∞	6	12	13	14	15	17	18	119		

DEVICE B" DATA SHEET

MOTES: (a) $-\frac{1}{2}$ = 1 aspers (b) $-\frac{1}{2}$ = 500 asperve

		dda	Τ.					1
		1	-	<u> </u>			1	
Date 30 April 1963	Ty = 125°C ± 3°	d(T)		ı	•	•		
ri1	25%		8	00	00	700		
0 Ap	1,	toff / Tapp	>1001000	>100 900	>100 300	>100 7		
2		E I	7					
শ্ৰ	-	I.	52	110	108	110		
	1 30	a a						
	Ty - 25°C ± 3°	ļ	2	2 12	- 2	7		
	1 m	* (§	1.9	2.2	2.5	1.9		
	-	F-1	7 85	1 96	8 86	85		
		T VCT	2 D. 7		7 b.8	0.8		
•		T ₂	12	45	27	25		
DATA SHEET	0	(ER)FO or 1FO	10	25	25	25		
	- 125°c ± 3°	V(BR)FO or VFO	1200	1000	420	840		
1.81.2	T, - 1							9
DEVICE"B"		1(BR)RC or 1RO	15	25	25	25		# # # # # # # # # # # # # # # # # # #
		(83) RO or RC	1200	1040	420	820		
						···		
		, V _{GT}	1.0	1.6	1.0	1.1		
		LGT	30	82	51	62	·	
		1(BR)FO or 1 _{FO}	0.4	10	10	10		
1	Ty = 25°C * 3°	*(BR)FO or *FO	1260	1000	420	098		
01	T, - 2		7	<u> </u>			<u> </u>	. !
BT-43 Control		1(BR)RO or 1RO	0.5	10	10	10		1 1 aspere 1 500 aspersa
BT-43		(BR)RO or "RO	1200	1080	420	840	•	1 1
કું			12	10	-			
lot 160.	1,	१ ३५५०		7	<u>۳</u>	4		EODS:

DEVICE'B" DATA SHEET

Parameters 2

1		2.		1	•		
		dd*_/	ļ-		· · · · · · · · · · · · · · · · · · ·		
963	or #	d(*)				·	
Bts 30 April 1963	Ty = 125°C ± 3°						
Apr	1	toff Tapp	800	800	<u> </u>		
8			17	23			
멅		Œ,	0	-	-		
	0	ı. H	200	200	160		
	Ty = 25°C ± 3°	ac a	•	2	9		
	2 - 5	,™	2.8	ب	2.2		
		P. 3	1.73	1.46	1.5		
		V _{CT}	1.0	0.8	0.8		
		LGT	30	28	19		
EI		<u>د</u>					
DEVICE'B" DATA SHEET	30	1(BR)FO or 1FO	25	25	25		
DATA	Ty = 125°C ± 3°	*(BR)FO or *FO	920	980	009		
IBI	, 12	*(B	6	- 	9		: 19
EDIA:		1(BR)RC or ¹ RO	25	25	25	·	TABLE 19
띰),	- 7		~~~		
		(BR)RO or FRO	880	076	580		
			1.4	٠٠,	_		
		T VGT		0.	2 1		
		LoT	69	39	45		
		¹ (BR)FO or 1 _{FO}	10	10	10		
	۳.						
sed	T, = 25°C ± 3°	V(BR)FO or VFO	1000	1100	620		
1£fu	7.						
BT-43 Au Diffused		1(BR)RO or 1RO	10	10	10		1, - 1 aspere 1, - 500 esperes
-43							
B2		(BR)RO or 'RO	1000	1080	909		 2
lot 160.		१ ३४५०	2	<u>—</u>	4		
4		L					-

DEVICE'B" DATA SHEET

Particular of the control of the con

lot N		BT-44 Control	1					DEVICE	DEVICE "B" DATA SHEET	A SHEET						ब	Date 30 April 1963	11 1963		
4		1,	. 3 - 25°C & 3°	١٠				i.	Ty = 125°c ± 3°	30			T.	Ty - 25°C ±	£ 3°		τ, τ _γ τ	t, 25c + 3°		
११ ३३५०	(BR)RO or RO	1(BR)PO or 1RO	*(BR)FO or *PO	¹ (BR)FO or ¹ 70	101	T _G T	(BB) FO or FO	(BR)RC or fRO	(BR)70 or or NO	1(BR)F0 or 1F0	Lot	T _O T	[™] (a)	, €	I. I.	I OH	In toes (Tapp	d(r _{FO})	/* _{AP?}	
1	1440	0	1400	0.01	·	,	1200	12	1220	10		,	•	•	•	'		2000	1000	
2	1440	5 6	240	9.	16	8.0	1200	10	280	25	∞_	0.6	0. 60. 781. 73	73 5	40	<u>'</u>	>1001000		•	
9	760		1420	0.01	17	8.0	1180	25	1200	10	7	0.7	0. 70. 761. 7		8	<u> </u>		2000	1000	
4	1400	2 5	1360	0.03	17	8.0	1200	15	1200	22	ω	0.6	0.60.781.9		8	<u>'</u>		3300	1000	
9	1400	2 22	1360	0.04	18	8.	1200	=	1200	25	<u>∞</u>	0.5	0.50.781.9	6	8	<u>'</u>	>1001000	'	•	
							<u> </u>													
	-														·	· • · · · ·	*******	• • • • • • • • • • • • • • • • • • • •		
																				
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																J. 40				
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		,																		
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			******													·····				
															·· · · · · · · · · · · · · · · · · · ·					
jë	3	1.5					1							-	1	\blacksquare			1	
		1 8 -	į					TABLE	20											

DEVICE "B" DATA SHEET

7

NOTES: (a) - $\frac{1}{7}$ - 1 supers (b) - $\frac{1}{7}$ - 50 super

					**													
	Ty = 125°C ± 3°	q(a)p	> 20	2500	> 20	1	,	•	•	•	•	•	•	٠	•	ı	1	
	- 125	8	I	1000	1000	1000	1000	1000	1000	1000	1000	1000	1000	1000	100p	1000	100 0	
1	T	toff App	28 1000	20	24 1	27 1	27 1	28 1	28 1	35 1	33 1	32 1	32 1	28 1	32 1	28 1	30	
		I BD							ED	ns.	WE	TOF	Į					
İ		I _{B0}	8	160	100	,	,	,	,	!	1		1	,	,	,	•	
	± 3°	*5. 8	®	<u>~</u>	<u> </u>	,	,	1	1	ı		1	1		,	,		
	- 25°C	, (g	7		<u></u>													
	T,	* (*)	1.332.4	4 2.7	3 2.8	<u> </u>	<u>'</u>	<u>.</u>	<u> </u>								<u>.</u>	
-		TD _A		.9 1.4	.7 1.3	'	· •	<u>'</u>	÷	'	<u>'</u>	÷	'	÷	.	.	.	17 - A. C. A. C. T. C. A.
		Lor V	43 1.2	28 .	$\frac{12}{}$													
			7			<u> </u>					<u> </u>		<u>.</u>			<u>.</u>		
	30	1(BR)FO or 1FO	70	10	25	21	17	14	14	6	13	20	6	25	11	10	22	
	- 125°C ± 3	(BR)FO or FO	1290	1200	1200	1200	1200	1200	1200	1200	1200	1140	1200	1160	1200	1200	1200	
	T,		-												· · · · ·	·		
		1 (BR) MC or or 1 MC	10	16	20	25	20	20	21	16	18	25	17	25	20	21	25	
		OH (NH)	260	1200	070	1160	1200	1200	1200	1200	1200	1080	1200	980	1200	1200	1120	
		,\$	1.5	1.2	1.0	1.1		1.3	1.7	1.1	1.1	1.0	6.	٥.	٥.	1.0	1:1	·
		,§	92	8	24	30	31	25	ጽ	21	22	22	17	27	25	32	35	
		1. (W) P .	10	.05	90.	10	10	10	г.	10	10	10	10	10	10	10	10	
	Ty = 25°C = 3°	Or (BR)	1440	1400	1260	1420	1440	1360	1360	1440	1380	1300	1400	1260	1420	1400	1360	
	, t	Care and a	21	10	10	10	10	-	m	1.5	.5	10	٠,	10	H	۲.	10	
		OHE SHE	1010	1580	840	1440	1440	1480	1480	1480	1480	1280	1480	120	1480	1480	1320	
	 	L	7	4	'n	11	12	13	14	15	16	17	18	19	20	21	22	

dia / (ala)

30 April 1963

DEVICE B DATA SHEET

BI-44 AU DIFFUSED

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000 000 1000

ie Ie		BT-45 AuDiffused	nsed					301 A 30	DEVICE "B" DAIA SHEET	1 सम्बद्धाः						Ā	ୀ ଆ	0 Apri	Date 30 April 1963	
- 41		•	T, - 25°C ± 3	36				L.	= 125°c ±	30				T, - 25°C	# 30	-		T, - 125°C *	25°C \$ 3°	
। भग्ना	OR (BR) TO OR OR	*(BR)BD or or 1BD	*(BR)FO or *FO	L(BR) PO or 1-ro	Į.	55	V(BR)RO or BD	1(BR)RC or 1-RO	*(BR)FO or or *FO	1(BR)FO or 1-FO	15	P. GT	p _g (g)	N 2	å å	J _B	i R	toff Tapp	QL gg	- F
1	1280	0.1	1280	90.0	15 1.	9.	1200	16	1200	15	9	1.0	1.35	2.2	6.5	8	 ^	>601000	2500	1000
7	1420	0.05	1400	6.0	7 0.	8.0	1200	10	1200	7	က	0.5	1.1	2.8	4.5	15		25 1000		1000
ю	1400	0.05	1420	5.0	22 1.	0	1200	15	1200	16	10	0.6	1.3	3.0	5.5	35		21 1000	3333	1000
4	1380	3.0	1160	5.0	28 1.	~	1200	ដ	920	7.5	12	1.1	1.16	3.0	6.5	25	NRE	45 1000	2500	1000
2	1400	9.0	1340	4.0	14 1.		1200	16	1180	11	7	0.7	1.27	2.7.5	5.0	23		50 1000	3333	1000
9	1420	0.05	1400	5.0	59 3.		1240	10	1200	6	23	2.4	1.17	3.0 8	8.5	19		27 1000	2500	1000
11	1360	0.04	1300	0.07	21 1.	_	1200	17	1200	17	6	0.73	1.28	3.0 4	4.0		ON			
12	1460	0.05	1320	0.5	72 4.	- 2	1200	10	1020	10	31	2.9	1.13	2.8 10	10.0				******	
ដ	800	0.01	1000	0.01	23 1.	m	1020	17	1080	25	6	0.831.	1.15	2.5 4	4.5					
14	1380	0.05	1340	0.03	16 0.	26	1200	14	1200	17	^	0.651.	73	3.3 4	4.0					
25	1420	0.05	1220	0.02	12 1.	0	1280	10	300	3.0	2	0.691.	7	3.1 5	5.0					
16	1400	0.04	1340	1.0	12 0.	0.95	1290	ដ	1200	10.0	2	0.60	0.641.2	2.6 4	4.5					
20	1400	0.01	1380	0.5	27 1.	9.1	1200	11	1200	10.0	11	1.0	0 1.3	2.8 7	7.0					
22	1460	4.0	1440	6.0	31 1.		1200	14.	1200	10.0	14	0.73	7,11.2	2.5 5	5.0 -1	-NOI-	<u> </u>	MEASURED	1	
23	1260	0.07	1360	0.4	19 0.	6.0	1200	22	1200	21	∞	9.0	1.1	2.3 5	5.0			· · · · · · · · · · · · · · · · · · ·		
24	1400	0.04	1360	0.06	20 1.	1.1	1200	14	1200	12	10	0.8	1.1	2.9	6.0	<u></u>	·			
23	1400	0.03	1380	0.04	16 1.	1.1	1200	01	1240	10	7	0.7	1.2	2.3 5	5.0					
28	1360	0.02	1400	0.3	15 0.	6.0	1200	17	1200	15	9	0.6	1.1	2.8 5	5.0					
31	1400	0.03	1360	0.05	13	0.85	1200	ដ	1220	.01	5	0.5	1.0	2.6 5	5.5					
32	1360	0.03	1360	2.0	19 1.	1.0	1200	70	1200	20	00	0.6	1.2	2.8 4.	٠.				•	
EF.	180	5.0	1440	0.3	30 11.5	5	200	10	1200	14	12	0.911.	1, 2 3	.2	٠,					
ECILIS:	:	5 - 1 aspare											1]
	+ · -	4 - 500 mperve	į				• '	TABLE 2	22											

NOTES: (a) — $I_p = 1$ asperv (b) — $I_p = 900$ aspervs

۱										-	Ì					
	T, = 25°C ± 3°				TJ	= 125°C ±	30			r _J	25°C ± 3°			1,1	• 125°C ± 3°	
1 (BR) NO.		1(BR)FO or 1-FO	Ler Ver	W(BR)RO or ARO	1(BR)RC or 1RO	*(BB)70 or *FO	1(BR)FO or 1FO	for	A LD A	(a) (b)	o o	Œ.	ι Ω	toer / Tapo	d(*)	dda /
1.4	076	0.01	10 1.0	0 1260	10	096	3.0	7 0	0.7 1	1.12.6	5.0			·········		
0.07		10.0	24 1.	1 1180	25	1120	25.0	10 0	0.8 1	1.3 2.8	8,0				······································	
0.02		1.0	40 2.0	0 1100	25	1100	25.0	16 1		1.5 3.0	0 7.0					
0.1		0.02	15 1.0	0 1125	25	1140	25.0	9	63	1.2 2.7	5.0					
0.1	1360	0.07	50 0.9	9 1400	10	1220	3.0	25 0		1.1 2.6	<u>ئ</u> ن			··· .		
0.03	1360	0.05	17 0.95	1200	15	1200	14.0	7	0.6	1.1 2.8	5.0					
0.04		1.2	19 1.1	1200	15	1200	15.0	<u>о</u> ∞	72	1.33.	0 5.5					
0.05		10.0	19 1.0	0 1200	15	840	0.6	<u>o</u> 8	0.7	1.2 2.	7 5.2	·				
10.0		0.1	22 1.0	0911 0	25	1200	14.0	6	0.7	نا	9.5	-	2			
0.05	1360	0.4	10 1.0	1200	23	1140	14.0	4	0.63	1. 2 2.	4.8		587	MEASURED	TEN.	
0.03		0,03	22 1.1	1 1080	25	1080	25.0	6	0.7	1.0 2.	5.0				<i>j</i>	<u> </u>
0.02	1360	0.02	16 0.	95 1200	1.5	1200	12.0	7	_	1.0 2.	6 5.5					
0.05		0.02	20 0.85	84 1200	11	1240	10.0	8	0.60	0.952.	4 5.8					
0.05		0.13	16 0.9	9 1200	14	1240	9.0	<u> </u>	0.60	0.97 2.	5.0					
0.05		0.08	12 0.8	8 1200	7	1220	0.9	2	0.551.2	.2 2.	5.8					
0.04		0.07	11 0.85	85 1200	10	1260	10.0	4	0.6 1.	1.1 2.	5.0					
			······································													
														·		<u> </u>
				,	,											
	<u>.</u>															

Date 30 April 1963

DEVICE "B" DATA SHEET

TABLE 24

		dd* /	100	1000			· <u></u>	·····								7	
1963	°C # 3°	١ ـ .	2000						(20 00					·····			
Dete30 April 1963	Ty = 125°C ± 3°	toff / Tapp	>100 100C	>100 1000												_	
7		H ₂					<u></u>	····					····	- 1		-	
ă	-	I GE						·		· · · · · · · · · · · · · · · · · · ·	***************************************					-	
	5°C ± 3°	a g	4	4		·····			-··· , · <u>.</u>				*****				
	Ty - 25°C ±	'₂ ®	1.5	1.7			·									1	
		Þ . €	0.8 1.5	0.781.7								· · · · · · · · · · · · · · · · · · ·			······································	1	
		*GT		1													
		To.		t	· · · · · · · · · · · · · · · · · · ·		 										
Lahs	0_	(BR)FO or 1FO	25	10													
DEVICE "B" DATA SHEET	T, = 125°c ± 3°	*(BB)FO or *FO	1200	1200				•						*******			TABLE 24
DEVICE	1. P.	1(BR)RC or ¹ RO	16	14											*************************************		TA
		V(BR)RO or VBC	1200	1200						P		* · · · · · · · · · · · · · · · · · · ·		***************************************	100 B 2		
		VGT	1.0	1.0				*			******						
		Lor	22	15													
		1(BR)FO or ¹ FO	0.05	10.													
	T, = 25°C ± 3°	V(BR)FO or VFO	1310	1250													2
Control	£	1(BE)RO or 1 _{BO}	0.5	0.2	***************************************											1, - 1 amore	<u> </u>
Lot 16. BT-46		(BR)RO or ND	1360	1380												3 5	
is is	41	(३१५५)	1	7												is and a	

DEVICE "B" DATA SHEET

1		Q. I	<u> </u>	8	8									1
		dd'e /	009 (2500 1000	3300 1000			<u> </u>			***	· · · · · · · · · · · · · · · · · · ·		
1963	°C = 3°	d(vpo)	860	2500	3300									
Ats 30 April 1963	Ty = 125°C ± 3°	toff Tapp	009	1000	1000									•
30 A		t off'	1.5	30	18									
Pite		^I B0	ı	1	1									
		I, BD	1	1	ı	·								
	Ty . 25°C ± 3°	o o o	6.5	3.4 10.0	8.0									
	1.	(a)	. 864.4	3.4								,		
		ν _F (ε)	1.86	1.7	2.1									
		VGT	•	ı										
		r _{er}	ı	t	1									
SHEET		¹ (BR)FO or ¹ FO	10	13	20									
" DATA	Ty - 125°C ± 3°	(BE)FO or FPO	900	1200	1200			·····	, , , , , , , , , , , , , , , , , , , 	<u> </u>				
DEVICE "B" DATA SHEET	T,	1 (BR)RC or 1 RO	15	7	25								<u></u>	
H		(BR)RO or NBO	1200	320	1200									
	-	g.	1.6	4.0	2.1									1
			40	74 4	75 2									1
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net.	Ty - 25°C & 3°		-		,	· · · · · · · · · · · · · · · · · · ·							···-	1
Eusec	52 - 25	,	1170	1320	1320	<u></u>							<u>·</u>	
BT-46 Au Diffused		1(BR)HO or 1ED	0.05	0.05	0.05									1, - 1 aspere 1, - 90 esperes
BT-46		Og (BE)	\vdash	370	1400									35
lot 180.		H STUN		2	m									Ë

DEVICE "B" DATA SHEET

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E50GXI4-SI

RECTIFIER COMPONENTS DEPARTMENT

ON-VOLTAGE TEST, HIGH LEVEL SCR AND LIGHT ACTIVATED SWITCH

COMMUNICATIONS MUST SPECIFY COMPLETE NUMBER

A. GENERAL

On-voltage (formally called forward voltage drop, conducting state) of a controlled rectifier is an extremely important parameter in establishing the current vs. temperature rating of the device. Measurements of on-voltage are usually made at two current levels. The high level test is made in the region of the forward characteristic where the voltage drop is primarily determined by the effects of resistance of the device including the pellet, back-up plates, solder joints, tubulation joints, terminals, etc.

B. PROCEDURE

This test is normally performed at room temperature ambient. In order to prevent excessive junction heating, a single pulse of current shall be used, approximately half sine wave in shape and with a specified base width. In order to eliminate errors caused by the effects of resistance in the power supply circuit, the voltage measurement shall be made by employing four point connections (separate voltmeter and current connections to each terminal). The location of the voltmeter connections shall be as specified. Care must be taken to eliminate ground loops within the equipment. The voltage measurement shall be made at the peak of the voltage waveform that occurs at the same point in time as the peak of the current pulse. If a distinct peak on the voltage waveform does not occur at the same time point as the peak of the current waveform, erroneous readings will result. For controlled rectifier testing the device may be either triggered from a separate gate supply or from the anode by means of a resistor connected from gate to anode terminals. For light activated switch testing the device may be triggered from any appropriate light source. For either SCRs or light activated switches extreme care must be taken to eliminate the effects of zero shift on the device voltage measurement caused by the presence of triggering signal when the voltage measurement is made.

C. TEST CONDITIONS

To perform this test, the following conditions shall apply unless superceded by the product test drawing.

1. Fixed

(a) Forward Current Pulse Shape

Half Sine Wave (approx.)

(b) Forward Current Pulse Base Width

max. 4.0 m sec.

min. 0.5 m sec.

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RECTIFIER COMPONENTS DEPARTMENT

TEST METHOD

ON-VOLTAGE TEST, HIGH LEVEL SCR AND LIGHT ACTIVATED SWITCH

COMMUNICATIONS
MUST SPECIFY
COMPLETE MIMBER

			SCR AND LIGHT ACTIVATED SWITCH	COMPLETE NUMBER
c.	TES	T COI	NDITIONS (Cont'd)	
	2.	Var	iable	
		(a)	Temperature (Specify Case or Ambient)	°C (±5°C)
		(b)	Peak Forward Current	_Amperes (±2%)
		(c)	Gate Trigger Pulse (SCR) volts (±50%) and	ohms (±10%)
		(d)	Effective Light Trigger Intensity (Light Triggered Switch) Minimum	watts/cm ²
			Maximum	watts/cm ²
		(e)	Location of Voltmeter Connections Anode:	
			Cathode	
D.	TES	1. 2.	Factory Volts Peak Max. Customer Volts Peak Max.	

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RECTIFIER COMPONENTS DEPARTMENT

TEST METHOD

ON-VOLTAGE TEST, LOW LEVEL SCR AND LIGHT ACTIVATED SWITCH COMMUNICATIONS MUST SPECIFY COMPLETE NUMBER

A. GENERAL

On-voltage (formerly called forward voltage drop, conducting state) of a controlled rectifier is an extremely important parameter in establishing the forward current vs. temperature rating of the device. Measurements of on-voltage are usually made at two current levels. The low level test is made in the region of the forward characteristic where the voltage drop is primarily determined by the effects of the junctions only and, as predicted by theory, generally follows a logarithmic relationship with the current. Since SCR's exhibit more than one state of conduction, it is necessary to establish the lowest conduction state (lowest on-voltage) by means of an anode current pulse prior to voltage measurements.

B. PROCEDURE

SCR's and Light Activated Switches -

This test is normally performed at room temperature using the waveforms shown below. In order to minimize junction heating, the width of the initial pulse must be limited and the voltage measurement should be made between 30 milliseconds and 5 seconds after the start of the initial pulse.

The device under test is to be switched to the on-state by using the specified trigger pulse or light intensity. The trigger pulse width shall not be less than 10⁻⁵ seconds or more than 10⁻⁵ seconds. The specified gate bias conditions shall be observed during the measurement interval. Four point connections (separate voltmeter and current connections to each terminal) shall be used to minimize errors due to contact resistance.

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FORWARD CONTRENT WAFEFORM

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RECTIFIER COMPONENTS DEPARTMENT

TEST METHOD

ON-VOLTAGE TEST, LOW LEVEL SCR AND LIGHT ACTIVATED SWITCH COMMUNICATIONS MUST SPECIFY COMPLETE NUMBER

c.	TES	ST CONDITIONS
	To	perform this test, the following conditions shall apply unless perceded by the product test drawing:
	ı.	Fixed
		a. Test Time, minimum 30 m sec.
		b. Initial Forward Current Duration, Minimum 0.1 m sec. Maximum 10 m sec.
	2.	Variable
		a. Temperature (specify case or ambient)°C (±5°C)
		b. Test Current mAdc (±2%)
		c. Gate Trigger Pulse volts (±50%) and ohms (±10%)
		d. Effective Light Trigger Intensity (Light Activated Switch)
		Minimum w/cm ²
		Maximumw/cm ²
		e. Initial Forward Current, i _{f1} A (±5%)
D.	I	ST LIMIT
	ı.	Factory Vdc max.
	2.	Gustomer Vdc max.

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E50GX28-51

RECTIFIER COMPONENTS DEPARTMENT

TEST METHOD

SCR EFFECTIVE THERMAL RESISTANCE

COMMUNICATIONS MUST SPECIFY COMPLETE NUMBER

A. GENERAL

Faulty processing such as poor solder wetting will increase the thermal resistance from junction to stud. An upper limit on Θ J-C is necessary in order to keep junction temperature within the published limit for rated operating conditions.

The temperature dependence of the on-voltage with the low level current flowing is used to measure junction temperature rise while a constant power is being dissipated under constant cooling conditions.

B. PROCEDURE

The SCR shall first be completely switched on with a high level forward current pulse approximately equal to rated value and of 10^{-5} to 10^{-1} seconds duration which is then lowered to a low level dc metering current of negligible heating value. The on-voltage $V_{\rm FO}$ is then measured.

The device is then heated with a forward current which is interrupted periodically for measurement of on-voltage with only the low level metering current flowing. Heating watts shall be maintained constant during the heating time. Devices rated 50 amps and above should be water-cooled with a constant flow of cooling water in order to permit reaching thermal stability in a reasonably short time.

After a specified heating time, the on-voltage measured during the intervals when only the low level metering current is flowing is compared with the previously measured low level on-voltage (before application of heating current). The voltage decrease shall be no greater than the specified limit. The forward current shall be lowered without interruption to the low level metering value at the end of the heating interval, and the on-voltage observed. If the on-voltage does not return to the value measured just prior to application of heating current, the test shall be re-run without interruption of low-level metering current. In other words, if the low-level on-voltage does not return to the starting value, there has been a change in conduction state and the test should be re-run without interruption of forward current.

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C. TEST CONDITIONS

To perform this test, the following conditions shall apply unless superseded by the product test drawing.

1. Variable

A .	Low	level	meteri	lng	current
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RECTIFIER COMPONENTS DEPARTMENT

TEST METHOD

SCR EFFECTIVE THERMAL RESISTANCE

COMMUNICATIONS MUST SPECIFY COMPLETE NUMBER

; .	TEST CO	NDITIONS (cont'd)		
	ъ.	Forward heating current waveform (300° conduction with 60° interval for low level measuring current reading as in a 6-phase star circuit with one phase by-passed, has been found satisfactory).		
	с.	Forward average power		Watts ±5%
	d.	Heating time		sec ±1 sec.
	е.	Time interval between start of reference current interval and measurement of low level reference current on voltage		MS Min. MS Max.
	f.	Temperature sensitivity		mv/°C
	g.	Mounting torque or force	In. Lbs. or	Lbs.
	h.	Water flow rate		GPM ±10%

D. TEST LIMITS

- 1. Factory *
- 2. Customer *
 - * The test circuit readings are in millivolts change in low level on-voltage. This can be converted to thermal resistance in "C/W by multiplying the millivolt reading by the appropriate conversion factor. This reading will be thermal resistance from junction to cooling medium. True thermal resistance junction to case will be less by the amount of case to cooling medium thermal resistance.

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RECTIFIER COMPONENTS DEPARTMENT

TEST METHOD

SCR TRANSIENT THERMAL IMPEDANCE

(LARCRATURY TEST)

COMMUNICATIONS MUST SPECIFY COMPLETE NUMBER

A. GENERAL

The measurement of effective thermal impedance is included in the measurement of transient thermal impedance outlined below, since it is the steady-state valve of the curve of transient thermal impedance.

The thermal capacity of the various materials used in the construction of a semiconductor device precludes the use of effective thermal impedance in predicting device performance under transient conditions. The response of junction temperature to a constant power input, as a function of time, provides a curve of transient thermal impedance which can be used for this purpose.

B. PROCEDURE

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The transient thermal impedance of an SIR may be measured by utilizing the temperature dependence of the on-voltage. The valve measured is that between junction and ambient (cooling medium) for a particular heat sink and cooling medium flow. Transfert thermal impedance from junction to case cannot be measured directly, since the case temperature will change during the test, but can be interpolated, as shown in the figure. The measurement may be made by the heating method or by the cooling method:

1. Heating or Pulse Method

Measure the on-voltage $V_{\rm Fl}$ with a low level metering current flowing and with the junction at various specified temperatures. The measurement shall start with the highest temperature recommended by the manufacturer and shall be preceded by conduction of a high level of forward current which is lowered smoothly to the metering current, to insure a fully switched condition. Plot on voltage $V_{\rm Fl}$ against junction temperature and calculated slope (M) in volts per degree centigrade. Any large steps in the curve will invalidate the use of the slope (M).

Heat the device with a pulse of pure dc current and measure the peak power $P_{\rm Fl}$. At the end of the pulse record the on-voltage $V_{\rm F2}$ with the low level metering current flowing. The transient thermal impedance from junction to cooling medium for the time corresponding to the particular pulse duration is then calculated from:

$$\Theta_{\text{U-A} (t)} = \frac{(V_{\text{F2}} - V_{\text{F0}})}{(M) P_{\text{F1}}}$$

Where (M) = V_{R1}/T_{T} from the previous plot.

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RECTIFIER COMPONENTS DEPARTMENT

TEST METHOD SCR TRANSIENT THERMAL IMPEDANCE

(LABORATORY TEST)

COMMUNICATIONS MUST SPECIFY COMPLETE NUMBER

 ${\bf V}_{{\bf F}0}$ is the on voltage at the metering current level just prior to application of forward heating current. (Junction at cooling medium temperature).

 $V_{p,2}$ is the on voltage with the metering current flowing immediately following the heating current pulse. *

Repeat with current pulses of different time duration until enough points are obtained for a plot. See Fig. 1.

* This measurement must be made with an oscilloscope and the trace extrapolated back to the time corresponding to the end of heating current pulse. The extrapolation must exclude non-thermal transients such as recovery voltage and the effects of iron in the housing. When using this pulse method the junction must be allowed to cool back to equilibrium temperature between pulses. An off-time of at least 100 times the pulse width shall be used.

2. Cooling Method

As an alternative test procedure, the low-level on-voltage at the end of the current pulse of sufficient duration to bring the device to thermal equilibrium may be monitored until the device has cooled to thermal equilibrium under constant cooling donditions. An oscilloscope shall be used to record the beginning of the cooling cycle, and manual readings with a stop watch may be used after the cooling rate has slowed sufficiently. Calculations are the same as in the pulse method above, except that the value of transient thermal impedance calculated corresponds to the time interval between switching and the reading of $V_{\rm F2}$.

Since this is a cooling cycle, the calculated values of transient thermal impedance must be subtracted from the effective thermal resistance (the value calculated for the time when the forward heating current is cut off).

The advantages of this cooling method are:

- 1. Simpler circuitry.
- 2. Any discontinuities due to imcomplete firing are readily seen.

The disadvantages are:

- 1. The necessity for a calibrated oscilloscope and attached camera.
- Plotting from the pictures is tedious and may be inaccurate due to parallax or insufficient amplification of the trace

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TEST METHOD SCR TRANSIENT THERMAL IMPEDANCE

(LABORATORY TEST)

COMMUNICATIONS MUST SPECIFY COMPLETE NUMBER

2. Cooling Method (cont'd)

The cooling method shall be used on large devices, particularly for times of 1 second or longer. The heating method offers the greatest accuracy at the short time end of the curve and shall be used on all small devices (up to 50 amperes rating).

C. TEST CONDITIONS

To perform this test the following conditions shall apply unless superseded by the product test drawing:

- 1. Variable
 - a. Low level metering current

A ±2%

b. Forward heating current

(usually 50-100% rated current for cooling method, higher for short pulses in heating method).

A +97

c. Method of extrapolation of scope trace back to time when forward heating current is cut-off.

D. TEST LIMITS

Specify time intervals to be checked and transient thermal impedance limit values (Factory and Customer).

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